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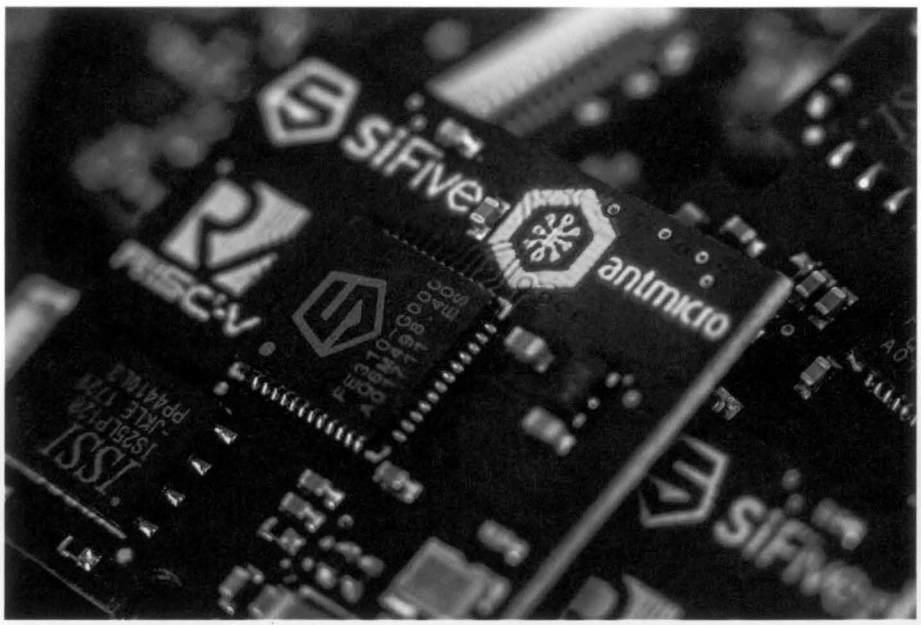
Will RISC-V Revolutionize Computing?

The open instruction set for microprocessors promises to reshape computing and introduce new, more powerful capabilities.



Modern computing depends on many components to deliver fast speeds and high performance, yet few play a more integral role than a *reduced instruction set computer*, commonly known as RISC. Although the instruction set architecture (ISA) comes in different shapes and forms—and it supports numerous systems and devices—there is a common denominator. RISC allows microprocessors to operate with fewer cycles per instruction (CPI) than a complex instruction set computer (CISC).

An ISA is at the heart of computing, of course. "It is the basic vocabulary that allows hardware and software to communicate," says Dave Patterson, professor of computer science at the University of California, Berkeley, and an ACM A.M. Turing Award recipient who essentially coined the term and developed early RISC computing models. Over the last couple of decades, two major entities, Intel and ARM, have largely controlled ISAs. Their proprietary microprocessors run everything from laptops to cloud servers, and smartphones to Internet of Things (IoT) devices. Today, it's difficult to find a computing device without Intel or ARM processors inside.

All of this is about to change. A free, open instruction set called RISC-V, conceived by Patterson and fellow Berkeley professor Krste Asanović, along with their students, is turning the microprocessor industry upside down. The royalty-free ISA, which debuted in 2011, supports new and more specialized microprocessor designs that soon will appear in traditional computing devices as well as wearables, home appliances, robotics, autonomous vehicles and factory equipment. The appeal? "RISC-V delivers a very high level of flexibility at a much lower cost than proprietary RISC. It allows users to produce custom chips suited to specific applications," Asanović explains.

Following Instructions

The introduction of RISC-V coincides with other major changes in the semiconductor industry. It's no secret that CMOS transistor scaling is slowing. Even with recent breakthroughs in design that push density and performance to new levels, Gordon Moore's longstanding prediction of doubling transistors every two years—"Moore's Law"—no longer holds. As semiconductor advances slow—while performance demands continue to grow—the ability to design more advanced computing devices and fuel innovation is threatened. "Moving forward, the logical path is to add extensions to the basic instruction sets on microprocessors for application domains," Patterson explains.

The appeal is of RISC-V is undeniable. A common ISA means that different implementations and use cases for the ISA can tap the same core software stack, thus minimizing porting efforts to compilers, operating systems, and other software. The main advantage of RISC-V is not that it is a new variation or iteration of RISC, but that it is an open ISA. Hence, there's an expectation that the model will produce the software stack needed to put RISC-V on the commercial map. Yet, at the same time, there is also a fear that giving users the ability to alter the ISA will lead to a balkanization of the RISC-V software ecosystem.

Asanović and Patterson began working on the fifth-generation RISC instruction set in Berkeley's Parallel Computing Lab (Par Lab) in 2010. The project was born out of frustration over the lack of flexibility with proprietary ISAs. "We couldn't do some of the research we wanted to do," Patterson recalls. The pair took aim at a persistent industry problem: an inability to customize chips for specific purposes. The initiative was rooted in their own needs. "Since we couldn't get permis-

sion from Intel or ARM to use or modify their proprietary instruction sets, we decided to develop our own instruction set for our own research and to help the research of fellow academics."

The project caught the collective eye of the computing industry, and, with $10 million in lab funding from Microsoft and Intel and additional funding from DARPA, blazed forward. "It became apparent that many people wanted something akin to a Linux operating system for microprocessors. People desired an open instruction set that would allow anyone in the world to build chips using an open and common vocabulary," Patterson says. In 2014, RISC-V made its official public launch and, by then, the idea had garnered enough momentum to spawn the nonprofit RISC-V Foundation (riscv.org), which serves as a clearinghouse for research, standards, and industry collaboration. It now boasts more than 425 members.

Over the last couple of years, RISC-V has crept into mainstream computing. For example, Samsung announced that it will use RISC-V cores in its 2020 5G smartphones. The electronics giant also will tap RISC-V cores for artificial intelligence (AI) image sensors, security management, AI computing, and machine control systems.

Others are following suit. Western Digital, NVIDIA, and Qualcomm also have announced that they will use RISC-V for applications ranging from solid-state drives (SSD) and hard-disk drives (HDD) to graphics processing units (GPUs) used for smartphones and machine learning.

Reducing RISCs

The appeal of RISC-V is clear. "It opens entirely different possibilities through a modular design that allows users to add specific extensions based on specific computing needs," says Calista Redmond, CEO of the RISC-V Foundation. "The design bypasses a one-size-fits-all approach with prepackaged features and capabilities that you may or may not require—and the performance and energy drain that come with them." No less important, RISC-V wrestles control of microprocessors away from dominant industry giants Intel and AMR. "Instead, you have a diversity of suppliers and the innovations that come with them," she adds.

"Companies can build their own core to fit their own needs. They can have greater visibility into how the core runs, and even develop their own security features."

The result will be chips designed, built, and optimized for specific tasks. "There is nothing in the design that limits the application domain," Asanović explains. For instance, a RISC-V chip might be used to focus on a specialized AI task such as image recognition or machine language translation, or it could be used to establish a microcontroller framework that spans generations of devices and products. This would allow a business to bypass future R&D, as well as ongoing licensing and royalty requirements. "Companies can build their own core to fit their own needs. They can have greater visibility into how the core runs and even develop their own security features," he says.

In fact, many predict RISC-V will emerge as an industry standard. While RISC-V won't replace proprietary RISC, its custom extensions will enable entirely new types of applications, capabilities, and perhaps even devices. Says Asanović, "No longer will businesses be forced to adapt to the features of a chip. They will create a chip that matches their specific needs." Adds Abhi Shelat, an associate professor of computer and information science at Northwestern University, "In terms of use and cost for lower-end processors, this chip might dominate because of open-source economics. As the toolchain becomes a standard, it will be cheaper than using proprietary alternatives for many tasks."

Processing Change

Not surprisingly, RISC-V has doubters and naysayers. Critics argue the standard could introduce interoperability

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TOWARD THE TOPOLOGY OF DATA ANALYSIS

"In college, I was required to take some programming courses, and I immediately knew this was my area," says Tamal Dey, a professor of computer science at The Ohio State University. Several years later, while studying for his master's degree, Dey was exposed to computational geometry, and realized this was the niche of computer science for him.

Dey graduated Jadavpur University in Kolkata, India, with a bachelor's degree in electronics. He earned a master's degree in computer science from the Indian Institute of Science, Bangalore, and completed his Ph.D. in computer science at Purdue University.

His career started with faculty positions at the Indian Institute of Technology, Kharagpur, and research scientist positions at the University of Illinois and the Max Planck Institute in Saarbruecken, Germany, before joining the faculty at The Ohio State University in 1999.

Dey's research focuses on computational geometry and topology, with applications in computer graphics, geometric modeling, mesh generation, and shape analysis. His current interest is in topological data analysis, which sprung from computational topology.

"Computational topology has two aspects. One is recognizing various mathematical structures that can be extracted out of shape and data, and the other is the algorithmic issues of extracting them," Dey says. "I am currently focusing on the algorithmic aspects because they truly offer an opportunity to marry classical mathematics with the new discoveries in algorithm designs."

Dey feels scale, noise, dimensions, time, and algorithmic space constraints will bring new algorithmic challenges, and new mathematics will be needed to resolve them. "I wish to address these issues," he says.

—John Delaney

challenges across different types of RISC-V devices and ecosystems. Industry fragmentation and potential interoperability issues could emerge as different versions of the ISA take shape. In addition, binary compatibility with certain types of devices, such as smartphones, could present problems. Many apps currently are coded to conform to ARM instruction sets. Likewise, the platform could encounter challenges in certain high-end cloud environments, where enormous resources are required to build systems that rival proprietary ISA designs.

There are also questions about how the instruction set will evolve—and, for now, a lack of powerful tools for managing the technology. The RISC-V Foundation is promoting advances through collaborative standards and protocols. However, success hinges heavily on ongoing cooperation. As a result, some industry players, particularly those that stand to lose the most from an open ISA range, have taken aim at the technology. For example, ARM set up an anti-RISC-V website in June 2018. It was taken down a few days after going live when staff at ARM objected to the tactic. Then ARM announced in November 2019 that it wa s opening up its proprietary instruction set for Cortex M cores so customers can tweak and customize instructions.

Nevertheless, RISC-V is rapidly taking shape. A November 2019 report from Semico Research Corp. predicts the market for RISC-V CPU cores will reach 62.4 billion by 2025—or about 6% of the overall CPU core business. "Companies are turning to RISC-V solutions for a wide variety of applications and to address a wide range of performance and volume requirements," says Semico president Jim Feldhan. Communications, transportation and industrial settings are particularly hot sectors for RISC-V. "The idea of developing more innovative and efficient chips is incredibly appealing," Feldman says.

Security could also emerge as a primary selling point for RISC-V. Presently, there's no way to definitively know whether spyware or malicious code has been embedded at the BIOS level of a chip. "Today, microprocessor security is a black box," Patterson says. An open-source approach offers a couple of potential advantages. First, those using RISC-V chips would know exactly what is taking place on the microprocessor. Second, it would be possible for users to develop instruction set extensions and produce designs that focus on specific security needs. Companies and government entities could develop chips that are known to be free of embedded spyware or malware.

The future of RISC-V certainly looks bright. In addition to traction in the corporate world, more than two dozen universities are on board with RISC-V.

Powering the Future

The commercial introduction of RISC-V fills a longtime void in the computing industry, Redmond argues. Not only does it break the existing ISA duopoly of ARM and Intel, and allow users to take control of their own destiny, it establishes an open framework to fuel global collaboration and innovation. "It's a model that has demonstrated success over the last century in many different forms—from telephones and cars to networking and software," she says. "RISC-V represents a next logical phase of the concept and it is particularly suited to the IoT and an increasingly interconnected world."

The future of RISC-V certainly looks bright. In addition to traction in the corporate world, more than two dozen universities are on board with RISC-V. Not only are researchers looking to develop niche and boutique RISC-V chips to aid in their studies, schools including the University of California at Berkeley, the Massachusetts Institute of Technology, Cornell University, the University of Cambridge, and Tsinghua University in Shenzhen, China, have begun to develop educational materials and instructions related to the design, engineering, and use of RISC-V. "This is planting the seeds for more widespread adoption and greater use of the framework in the future," Redmond explains.

All of this will likely fuel a level of disruption the semiconductor industry has not witnessed in many years. Patterson has described the introduction of RISC-V as "a new golden age for computer architecture." Says Michael Taylor, an associate professor in the School of Computer Science and Engineering at the University of Washington in Seattle, "There are no serious technical or practical issues with RISC-V. It will eventually supplant x86 and ARM as the primary instruction set for microprocessors. It will fundamentally change the computing world." ■

Further Reading

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