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Design of Multiplexers using Reversible Logic Technique

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Abstract—Reversible logic is promising as it can be applied to different applications in low power like nanocomputing especially in quantum computing. Reversible logic is a technioue for power reduction. Reversible circuits are similar to digital circuits but they work using reversible logic gates. This study focuses on reducing the garbage output and ancilla inputs in reversible multiplexers, thereby reducing the power consumption. In this study two designs of Multiplexers are given. Design1 is using TwinSJ gate and AJ gate. 2:1, 4:1 and 8:1 multiplexers are built. In Design 2, a new gate (SJ gate) is built which functions as 2:1 multiplexer. It has 4*4 configuration. The inputs are suitably configured so that it performs various logic functions. Using this SJ gate and other basic reversible logic gates, 2:1, 4:1 and 8:1 multiplexers are built. In 2:1 multiplexer, Ancilla inputs are improved to '0' from 5 and garbage output has been reduced to 2 against 7 in existing design. 4:1 multiplexers are built with '0' ancilla inputs against 2 and 11 in existing designs. Garbage output of the proposed 4:1 multiplexer is 5 against 6 and 16 in existing designs. 8:1 multiplexer is built with 1 ancilla input and 11 garbage output against 2 and 12 respectively in existing design. This is designed using VHDL code - xilinx 14.7 for verification purpose and simulated on ISIM.

Keywords: Reversible logic, low power design, multiplexers, garbage output, ancilla input.

I. INTRODUCTION

Though reversible logic has traceability to year as early as 1973 by C.H. Bennett [1], recently Reversible logic is used in many areas due to its ability to design low loss or approximately loss less digital circuits. According to "Thermodynamics" traditional systems consume energy equal to KTln2 on loss of each it of data as stated by Rolf Landauer [2] in 1961. Here T is the temperature and K is Boltzmann's constant with value equal to $1.380649x10^{-23}m^2kg^2k^{-1}$(J/K) [3]. In 1973 C H Bennett correlated the heat loss with information lost. He stated that by reversible logic heat dissipation will be zero [4]. Compared to CMOS, nanotechnology saves more power [5]. This paper focuses on designing multiplexers using the new SJ reversible gate. VHDL coding for reversible gates using which complex circuits are designed. Nanotechnologies, especially Quantum-dot Cellular Automata (QCA), gives attractive perspective for future computing technologies [6].

Garbage outputs, gate count, quantum cost, Ancilla input are some of the cost factors in Reversible logic. Different methods for specific cost reductions may be established [7]. In this paper reducing ancilla input and garbage output are focused. Design and implementation of VLSI circuits using Reversible Logic Gates [8] is focused upon to reduce power by reducing the number of garbage outputs and ancilla inputs.

Some of the recent development areas mostly due to pandemic where reversible logic find its application are

- Internet of things (IOT)
- Remote sensing and contactless measurement
- Digital Ink
- online system testing and networking
- wearable computers

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II. REVERSIBLE LOGIC

A. Basics of Reversible Logic

Basic Reversible Gates are Feynman, Double Feynman, Toffoli Gate [9], Fredkin Gate, Peres Gate, TSG gate and Sayem Gate. There are gates built for unique applications. Reversible logic devices are used to reduce (theoretically eliminate) power consumption. In reversible logic circuits, number of inputs is equal to the number of outputs [10]. To achieve this ancilla inputs and garage outputs are used. These are not useful for the functioning of the gate. Some combinational circuits[11], D Flipflop, T Flipflop, decoders, latches and RAM cell are built with reduced GO and ancilla Input.

Reversible Logic has the following features

- Same number of outputs as that of inputs.
- Unique input to output pattern.
- Hardware complexity – A reduced model.
- Garbage outputs minimized.
- Gate count should be minimum.
- Constant value for inputs [‘0’ or ‘1’].
- Fan-out =‘0’
- Feedback or Loop back not allowed

Parameters in Reversible Logic Gates

- Quantum cost
- Garbage output
- number of Gates

Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for construction of arithmetic circuits used in quantum computation and other low power digital circuits [12].

B. Reversible Logic gates

There are different cost considerations in Reversible logic. Garbage outputs, gate count, quantum cost, Ancilla input are to name few [13]. Different methods for specific cost reductions may be established. In this paper reducing ancilla input and garbage output are focused. In modern digital world, low power design in both analog and digital VLSI circuits attracts more attention [14]. Design and implementation of VLSI circuits using Reversible Logic Gates [14] is focused upon to reduce power by reducing the number of garbage outputs and ancilla inputs [15]. Basic Gates used in this study are Feynman gate and FREDKIN Gate. Their block diagram are given in Fig.1. Feynman gate is used to avoid fan out. Fredkin gate is used for other functions. AJ gate has the functionality of AND and OR gate.

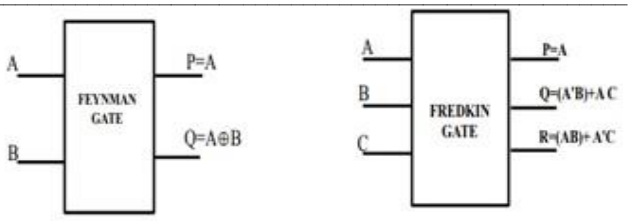

Figure 1. FEYNMAN Gate & FREDKIN Gate

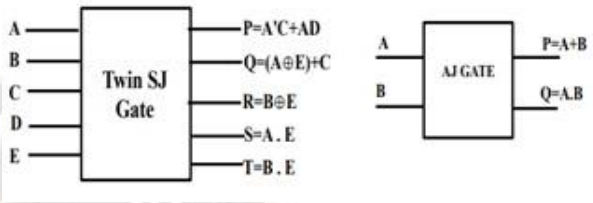

Figure 2. TWIN SJ Gate & AJ Gate

To build the circuit under study, SJ gate is designed and some basic reversible gates are used. By configuring the inputs properly, SJ gate can be used to perform some logical functions. SJ gate is used as a 2:1 multiplexer. Based on the state of A (0 or 1), either B or C is selected at output 'P'.

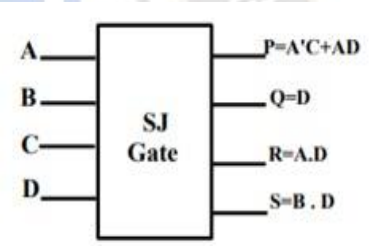

Figure 3. SJ Gate

TABLE I. TRUTH TABLE – SJ GATE

INPUT				OUTPUT			
A	B	C	D	P=A'C +AD	Q=D	R=A.D	S=B. D
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	0
0	1	1	1	1	1	0	1
1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0
1	0	1	0	0	0	0	0
1	0	1	1	1	1	1	0

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1	1	0	0	0	0	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	0	0	0
1	1	1	1	1	1	1	1

III. REVERSIBLE LOGIC IMPLEMENTATION

A. Related Study

Reversible Multiplexers using gates like Feynman, Fredkin, BJN and Peres gates. This design has more number of GO, CI and number of gates. In this work 4:1 multiplexer is built using different basic RL gates and BJN gate. It has 4 constant inputs and 10 garbage outputs. Using Feynman gate, Peres Gate and Fredkin Gates and a new BJN gate. This complicates the Fabrication, as different gates need to be integrated. A new reversible gate COG is built, which is used as 2:1 multiplexer. COG is a 3*3 Controlled Operation Gate. In this the authors have compared the conventional multiplexers with reversible multiplexers for Cost metrics and number of gates. Rather than Number of gates, quantum cost can be used as a metrics. Comparison of number of gates does not give clear picture about the chip area, as different gates occupy different area based on the number of Transistors used. Any reversible gate has many basic logic gates [16].

Fredkin gate is used as 2:1 multiplexer and focus is on fabrication. Previously researchers observed the system built 2:1 multiplexer, D Flip Flop and PIPO shift register using reversible gates. They have constructed the 2:1 multiplexer with 3 constant inputs and 8 garbage outputs. It is built using Feynman and Toffoli gates. Proposed study has a 2:1 multiplexer with 1 constant input and 3 garbage outputs. In the paper [18] 8:1 multiplexer is built using 4:1 multiplexer in which Fredkin gate is used as 2:1 multiplexer. In this design, though the authors claim 7 garbage output and 0 constant input actually 12 garbage outputs and 2 constant inputs are there. In the proposed design 8:1 multiplexer is built with reduced number of garbage outputs. 4:1 multiplexer is built in 2 approaches. One approach uses 3 TKS gates and other approach is with a VSMT gate. No of reversible gates used and Garbage outputs are compared for both approaches and confirmed that the second approach is better than the first one. Where a 8:1 multiplexer is built using 1 TKS gate and 2 VSMT gates. No of gates and Garbage outputs are the parameters verified [19].

A 4:1 multiplexer is built with 43 quantum cost, 11constant inputs and 16 garbage outputs. There is scope for reduction of garbage output and constant input [20]. In the proposed work it has been reduced to 0 constant input and 5 garbage output.

In this paper different Boolean functions are built using Feynman, Fredkin and Sayem gates. 4:1 multiplexer and D Flip Flop are built. Power, delay, GO and CI of the 4:1 multiplexer are compared with the existing design. The design has 6GO and 2 CI. This is reduced in the proposed design

B. Proposed Study

Reversible Multiplexer: Multiplexer is a data selector. Out of multiple inputs one is connected to the output. This selection is done by selection bits (S0, S1...). Out of 2^N input signals one input is selected using N select signals.

This work focuses on building multiplexers with less garbage output and less ancilla input. The authors propose two designs.

Design 1: In Design1 multiplexers are built using TWINSJ a 5x5 gate and AJ gate.

Multiplexer 2:1: TwinSJ gate acts as 2:1 multiplexer. Fig 4 shows the TwinSJ gate configured as 2:1 multiplexer. Output 'P'of the TwinSJ gate is the muxoutput of the 2:1 multiplexer. A is the selection bit and C and D are the inputs. B and E are the ancilla inputs and G1, G2 and G3 are the garbage outputs. Simulation results of 2:1 multiplexer are shown in **.

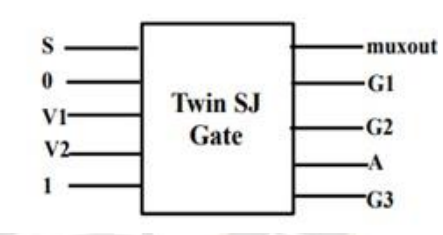

Figure 4. 2:1 Multiplexer using Twin SJ Gate

Multiplexer 4:1: The component under study is a 4:1 multiplexer. Multiplexer is a data selector. Out of various inputs one is selected to the output. This selection is done by selection bits. Out of 2^N input signals one input is selected using N select signals. Inputs may be Analog or digital signal. In this paper, 8:1 multiplexer is built using 4:1 multiplexers. 4:1 multiplexer circuit is built using three numbers of 2:1 multiplexer. 2:1 multiplexer is built using two FEYNMAN gates which is a reversible gate. FEYNMAN gate is a copier gate. If one of the inputs (B) is made 0, the other input (A) is available at both outputs. Output of a 4:1 multiplexer is

[(S0'.Vin1+S0.Vin2).S1'] + [(S0'.Vin3+S0.Vin4).S1]

Where Vin1, Vin2, Vin3 and Vin4 are input signals. Out of these, one signal needs to be connected or selected at the output. Two select signals S0 and S1 are available. In combination of 00, 01, 10 and 11, select signals can be configured to select Vin1, Vin2, Vin3 and Vin4 respectively.

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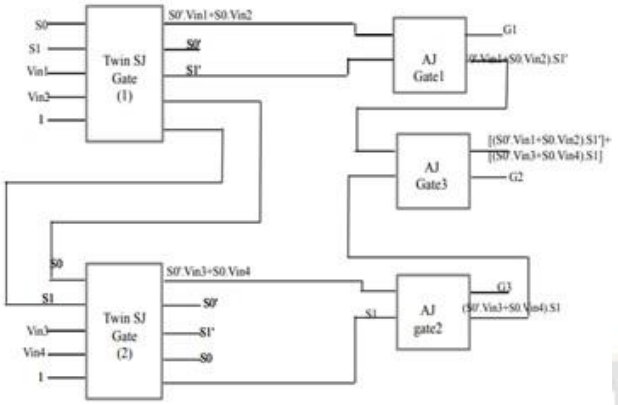

Figure 5. 4:1 Multiplexer using Twin SJ Block Diagram

Two TWINSJ gates and three AJ gates are used in 4:1 multiplexer. TWINSJ gate has the functionality of a 2:1 multiplexer and Feynman gates (repeater). In TWINSJ gate 1, When E input is High ('1'), s0 and s1 are available at S and T outputs. Vin1 and Vin2 are the inputs to TWINSJ gate1. Vin3 and Vin4 are input to Gate 2. AJ gate has the functionality of AND and OR gates. Output of AJ gate 3 is the selected output.

Muxout=[(S0'.Vin1+S0.Vin2).S1']+[(S0'.Vin3+S0.Vin4).S1]

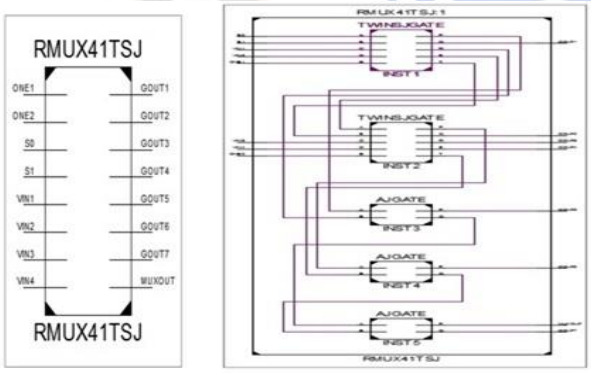

Figure 6. 4:1 Multiplexer using Twin SJ

Multiplexer 8:1: selects one out of 8 inputs. In this paper, 8:1 multiplexer is built using two 4:1 multiplexers and a TWINSJ gate. FEYNMAN gate is a copier gate used to repeat the signals as Fanout is not possible. If B is made as '0', then A is available at both output points.

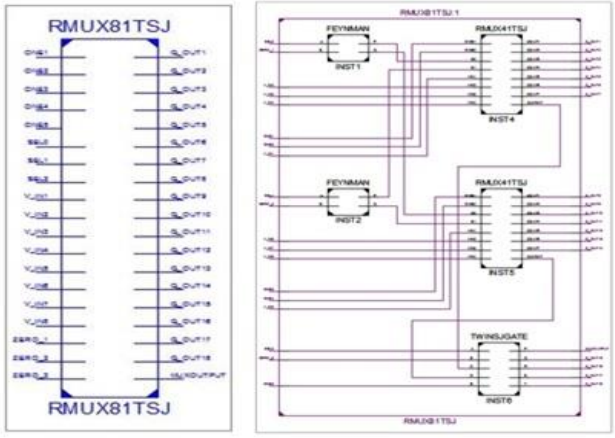

Figure 7. 8:1 Multiplexer using Twin SJ

Design 2: uses SJ gate and Fredkin gates to build multiplexer circuits. In the proposed design2 number of garbage outputs and ancilla inputs are reduced.

Multiplexer 2:1: SJ gate acts as 2:1 multiplexer. Fig 7 shows the SJ gate configured as 2:1 multiplexer. Output 'P'of the SJ gate is the muxoutput of the 2:1 multiplexer. 'P' is the muxoutput. P=A'C+AD where A is the selection bit and C and D are the inputs. C1 is the ancilla input and G1, G2 and G3 are the garbage outputs. Simulation results of 2:1 multiplexer are shown in Fig.6.

P=A'C+AD

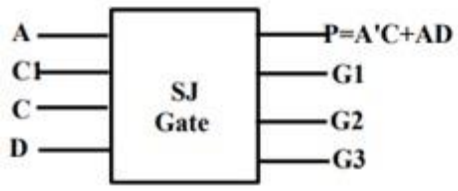

Figure 8. 2:1 Multiplexer using SJ Gate

Multiplexer 4:1: 4:1 Multiplexer is built using three SJ gates. Output of 4:1 multiplexer is

"Muxout=[(S0'.Vin1+S0.Vin2).S1']+[(S0'.Vin3+S0.Vin4).S]"

Where Vin1, Vin2, Vin3 and Vin4 are input signals. Out of these, one signal is connected or selected at the output. Two select signals S0 and S1 are available. In combination of 00, 01, 10 and 11, select signals can be configured to select Vin1, Vin2, Vin3 and Vin4 respectively. Three SJ gates are used to build a 4:1 multiplexer. SJ gate does the functionality of a 2:1 multiplexer. In SJ gate1, S1 is available at Q output as a repeater. Vin1 and Vin2 are the inputs to SJ gate1. Vin3 and Vin4 are inputs to SJ gate2.

Muxout=[(S0'.VIN1+S0.VIN2).S1']+[(S0'.VIN3+S0.VIN4).S1] is from the third gate.

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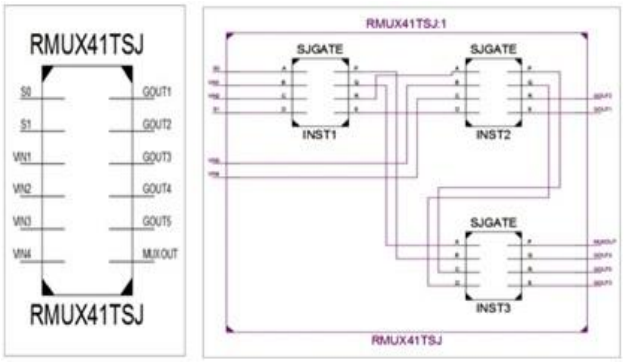

Figure 9. 4:1 multiplexer using SJ gate

Multiplexer 8:1: 8:1 multiplexer is built using SJ gates and FREDKIN gates. Eight inputs V_IN1 to V_IN8 are fed to SJ gates and Fredkin gates. Suitably using Feynman gates the select signals are reused. SEL0 and SEL1 are used in the circuit using copier gate (FEYNMAN gate).

Outputs of SJ gates are selected as "muxoutput" using a FREDKIN gate with SEL3 as the selection bit. Five SJ gates, one Feynman gate and two Fredkin gates are used. SJ gate acts as copying gate also. Some of the outputs are reused to reduce the ancilla inputs and garbage outputs.

Muxout=[(S0'.VIN1+S0.VIN2).S1'S2']+[(S0'.VIN3+S0.VIN4).S1S2']+[(S0'.VIN5+S0.VIN6).S1'S2]+[(S0'.VIN7+S0.VIN8).S1S2]

Various combination of selection signals are given and corresponding multiplexer output is noted. This has been verified and results are shown in the Fig.7. One ancilla input and 11 garbage outputs are used.

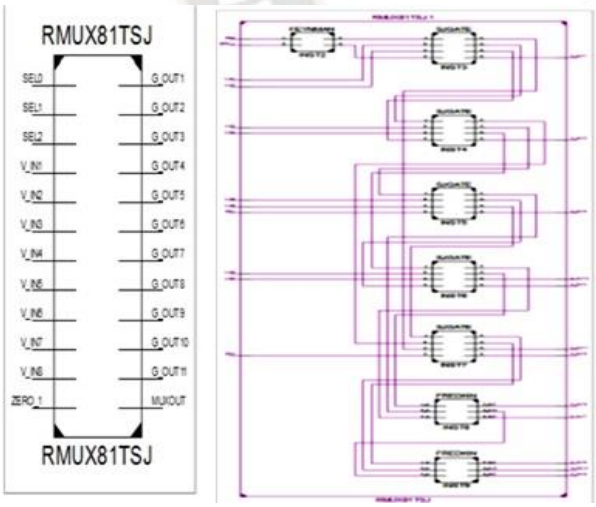

Figure 10. 8:1 multiplexer using SJ gate

IV. SIMULATION & RESULT

All circuits are coded on Xilinx tool using VHDL coding, simulated and verified for reduced garbage output and ancilla input.

A. Multiplexer 2:1

P output of SJ gate is the muxoutput of the 2:1 multiplexer. If A =0, B is selected at the output and if A = 1, then C is there at the output. Fig 6 shows the result.

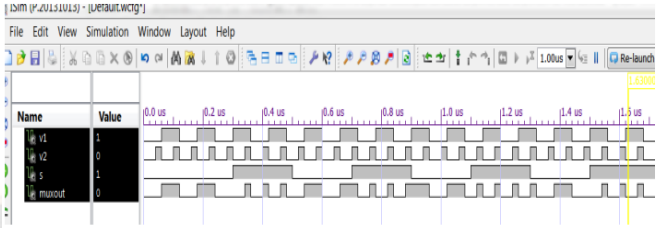

Figure 11. 2:1 Multiplexer Simulation Result

B. Multiplexer 4:1

In the sample, to show the results clearly, Vin1 is chosen as 100ns ON and 100ns OFF signal, Vin2 is 100ns ON and 20ns OFF, Vin3 is 20ns ON and100ns OFF and Vin4 is 40ns ON and 200ns OFF. In the fig.7 status of S0 and S1 at different timing and corresponding muxout can be checked. When S0='1' and S1='0', Vin2 is at the output, S0='0' and S1='1', Vin3 is at the output. When S0='1' and S1='1', Vin4 is there at the output.

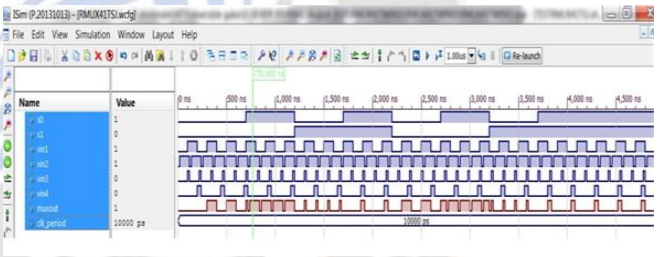

Figure 12. 4:1 Multiplexer Simulation Result

C. Multiplexer 8:1

Based on the 3 selection bits, one of the eight inputs is selected at the output. To show the difference in the output, signals with different timings are used. When SEL0, SEL1 and SEL2 are all 0, V__IN1 is available at the output. When SEL0 is made to '1' at 0.12 µsec, V_IN2 is selected at output. When SEL0 is made to '0' and SEL1 is made to '1' at 2.5 µsec, V_IN3 is selected at output. At 3.5 µsec, SEL0 and SEL1 are made to '1', V_IN4 is selected at output. Similarly for all combinations of selection bits, 100, 101, 110, and 111 the output is verified. At 7.5 µsec SEL0, SEL1 and SEL2 are '1' and V_IN8 is available at the output. Simulation results are shown in Fig.8.

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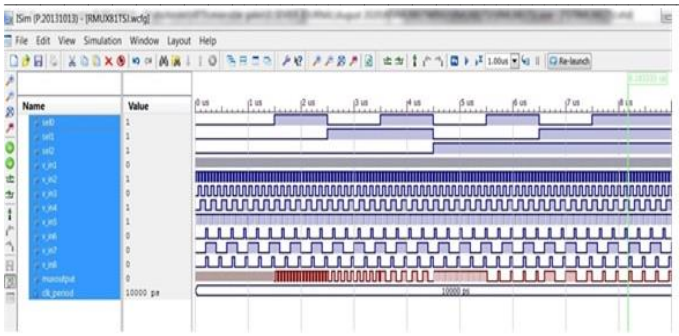

Figure 13. 8:1 Multiplexer Simulation Result

The table 2 shows the comparison Design1 and Design2. Table 3 shows comparison of various reversible multiplexers designed with the existing design. These designs are compared for Garbage output and ancilla input. Every proposed design is compared with the existing designs and improvement achieved are given. Fig.14 shows the results.

TABLE II COMPARISON OF DESIGN1 & DESIGN 2

Multiplexer circuit	Design 1		Design 2	
	Ancilla input	Garbage output	Ancilla input	Garbage output
2:1 multiplexer	2	4	1	3
4:1 multiplexer	2	7	0	5
8:1 multiplexer	8	18	1	11

TABLE III. COMPARISON OF ANCILLA INPUT AND GARBAGE OUTPUT

Multiplexer circuit	Existing design		Proposed Design		Improvement %	
	Ancilla Input	Garbage Output	Ancilla Input	Garbage Output	Ancilla Input	Garbage Output
2:1 Multiplexer[8]	5	7	0	2	100.00%	71.43 %
4:1 Multiplexer[14]	2	6	0	5	100.00%	16.67 %
8:1 Multiplexer[7]	2	12	1	11	50.00%	8.33%

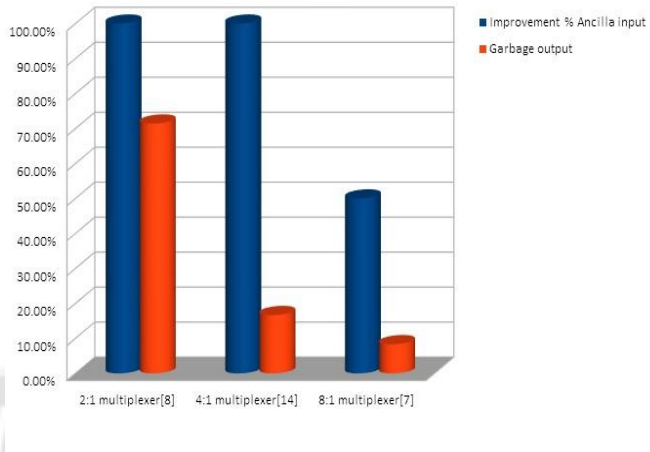

Figure 14. Comparison of Results

V. CONCLUSION

Reversible multiplexers of 2:1, 4:1 and 8:1 configuration are designed using Reversible Twin SJ gate (Design1) and SJ gate (Design2). Comparison with existing designs for garbage outputs and ancilla inputs shows the proposed design2 of reversible multiplexers are improved over the existing design in terms of garbage outputs and ancilla inputs. In the proposed design of 2:1, and 4:1 multiplexers using SJ gate there is '0' Ancilla input. 8:1 multiplexer is designed with 1 ancilla input. Similarly 2:1 multiplexer is designed with 2 garbage outputs (71.43% improvement), 4:1 multiplexer is designed with 5 Garbage outputs (16.67%improvement) and 8:1 multiplexer is designed with 11 garbage output (8.33% improvement). As multiplexer is an important element in CPU for selection of peripheral devices and memory accessing, this improvement will be helpful in design of low power computers and future system design

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None.

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