

A Modernistic Gate Clustering Technique to Depreciate Leakage in Cmos Circuits

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Abstract: Low power design is one of the most emerging paradigms in VLSI industry, since it is much important for hand held portable applications. As modern VLSI design emerges based on nanometer technology, power dissipation has become an important design closure parameter in ultra low submicron digital designs. Moreover, in CMOS logic circuits, the sub-threshold leakage current increases due to reduction in threshold voltage and voltage scaling which is most responsible for leakage power dissipation during standby mode and are increasing dramatically for every technology generation. Nowadays, this static power dissipation becomes a critical factor in low power design due to emergent mobile products. It means, the leakage power dissipation should be a major problem and it's a vital challenge for VLSI designers. In this paper, a new heuristic approach for clustering the logic gates in conventional CMOS design is proposed. Also, a power-gating scheme with the intention of diminishing leakage in idle mode is presented. The use of clustering will reduce the count of sleep transistor and the power gating helps more leakage savings in CMOS design. The proposed technique is tested on 4:1 multiplexer and 4 bit carry look ahead adder. Design and simulation were done on Tanner Tool 15.1 using CMOS nanometer technology.

Key words: Leakage Power • Power-Gating • Sub-threshold Leakage • Low power Design

INTRODUCTION

Nowadays, the most challenging circumstance for semiconductor device industries is to design low power high performance portable electronic devices. It is not due to the increasing demand of mobile applications alone. Even before the emergence of hand held devices, power consumption has been a fundamental problem in VLSI systems [1]. It is believed that for every technology generation, portable and battery-operated devices have to be developed with ultra-low power computational units. The current trend of shrinking the transistor size, diminishing the supply voltage and making more complex chip architectures have resulted in huge static power dissipation since trimming the threshold voltage due to voltage scaling leads to increase in the sub-threshold leakage current exponentially. It seems that, the leakage power is to be considered as a significant aspect in CMOS circuit design for every technology generation [2].

In order to design low power electronic devices, leakage power has to be reduced because static power accounts for the important portion of the total power

consumption in low power VLSI systems. To solve the static power dissipation problem, many researchers have come up with different ideas from the device level to the architectural level and have identified that greater than 60% of the total power consumption is due to the leakage phenomenon within which stand-by-leakage is another major component. The one and only source of power consumption in the static circuit is stand-by-leakage and it states that, the energy of fully charged device begins to lose, even if the device is not used for some period of time, which affects the lifetime and efficiency of the CMOS devices. Conversely, there is no universal way to avoid tradeoffs between power, delay and area and thus VLSI designers are still facing the massive challenge to satisfy the applications and product needs [3].

In CMOS design, the supply voltage and the threshold voltage have been continuously scaled down for every nanometer technology generation in order to achieve low power high performance devices. Nevertheless, leakage current increases exponentially due to scaling and turns out to be the first and foremost aid of the total power consumption. Furthermore, the static

power consists of both stand-by and active leakage currents. The dynamic and static power dissipation is expressed in terms of equations as shown [9] [1].

$$P_{dynamic} = \alpha f C V_{dd}^2$$

$$P_{static} = I_{Leak} V_{dd}$$

where α is the switching activity, f is the operating frequency, C is the load capacitance, V_{dd} is the supply voltage and I_{Leak} is the cumulative leakage current due to all leakage components. The total power dissipation is the sum of above two equations.

Finally it is illustrated that, static power dissipation is the significant portion of total power dissipation for current and future technologies. There are several low power design techniques introduced with the intention of reducing leakage power in digital CMOS circuits. In spite of every technique providing an efficient way to diminish leakage power, certain drawbacks of each technique limits the application. Generally, the leakage current consists of various components, such as PN junction reverse-bias current, sub-threshold leakage, gate leakage, gate-induced drain leakage and punch through leakage [4]. Among them the sub-threshold leakage is examined to be a major contributing component of the leakage power.

Thus, a new heuristic approach for grouping the logic gates in low power design with power gating is proposed. This technique limits the drawbacks as well as achieves more leakage savings with minimum delay which is far better than existing approaches.

MATERIALS AND METHODS

Efficient gate clustering Technique: As mentioned earlier, leakage power has evolved into an austere in nanometer CMOS technologies and there are efficacious techniques proposed with the purpose of shrinking leakage power in low power digital circuits. Conversely, plenty of drawbacks are faced by the circuit designers while targeting to diminish leakage in VLSI circuits. In this paper, an effective approach is initiated with clustering technique in order to trim leakage with less design effort.

Clustering Methodology: Clustering technique is one among the many efficient approaches to group the logic gates in the circuit design and it is also the most suitable method for VLSI designers with the intention of grouping gates in logic circuit [10]. Moreover, while using

clustering the circuit obtains easy way to determine the sub-threshold leakage without any complexity. Also, clustering helps to reduce the sleep transistor counts after finding the high sub-threshold leakage path in the circuit design since it is necessary to insert sleep transistor where the leakage is high so as to minimize sub-threshold leakage which leads to less static power. It is performed by assigning maximum leakage of sleep transistor as $250\mu A$ and then determining the sub-threshold leakage of all the gates in the circuit design and summing up the leakage current of gates in such a way to not as possible without exceed the maximum leakage current of sleep transistor ($250\mu A$). The proposed clustering algorithm for any conventional CMOS design is shown in Fig. 2.

Clustering algorithm can be described as follows: Assume 'n' be the total number of gates in any conventional CMOS circuit design $\beta\beta$ (28 gates in 4-bit CLA adder) and 'm' be the number of sleep transistors.

I_{subi} = Maximum sub-threshold leakage current of gate i

I_{max} = Maximum leakage of sleep transistor = $250\mu A$

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Create _ Clusters ( )
begin
    {
    design schematic of conventional CMOS circuit
    determine  $I_{sub}$  of all gates
    choose peak values of all  $I_{sub}$ 
    assign sleep transistor ( ST )
    max leakage =  $250\mu A$  ( $I_{max}$ )
    {
    loop:1
    sum all  $I_{sub}$  values  $\leq$  max leakage of ST
    create cluster 1 if total  $I_{sub} \leq 250\mu A$ 
    elsif  $I_{sub}$  of cluster 1  $\geq$  max leakage of ST
    remove gate's  $I_{sub}$  of Cluster 1 until  $\leq I_{max}$ 
    } }
Create n _ Clusters ( )
for all other gates in circuit
if loop :1 satisfies
form n_clusters
end cluster
Leakage_Reduction
determine max leakage of each clusters
choose peak values of each clusters in CMOS circuit
insert ST in any one of the cluster where  $I_{sub}$  is high
more savings in leakage
    
```

Fig. 2: Proposed Clustering Algorithm

The objective is to assign each I_{sub_i} to one cluster so that the total current in each cluster does not exceed I_{max} and the number of clusters used is minimized.

The mathematical formulation of the clustering heuristic is as follows:

$$\text{Clustering minimization, } C = \sum_{i=1}^n I_{sub_i}$$

subject to $\sum_{i=1}^n I_{sub_i} \leq I_{max} \quad i \in \{1, \dots, n\}$

where,

$$I_{sub_i} \begin{cases} \text{Cluster1} & \text{if } I_{sub_i} \leq I_{max} \\ \text{No Cluster} & \text{otherwise} \end{cases}$$

This model is completely based on Integer Linear Programming (ILP). The main focus is to form minimum number of clusters in CMOS circuit design. It should be noted that the total current of any cluster should not cross the maximum current limit of the sleep transistor, which is $250\mu\text{A}$. After forming cluster, power gating is used in any one of the cluster in the circuit design where the total current is too high. Here, two sleep transistors are used ($m=2$, one PMOS and one NMOS) in the cluster to minimize drain to source current (I_{ds}). The flow chart representation to form cluster is shown in Fig. 3.

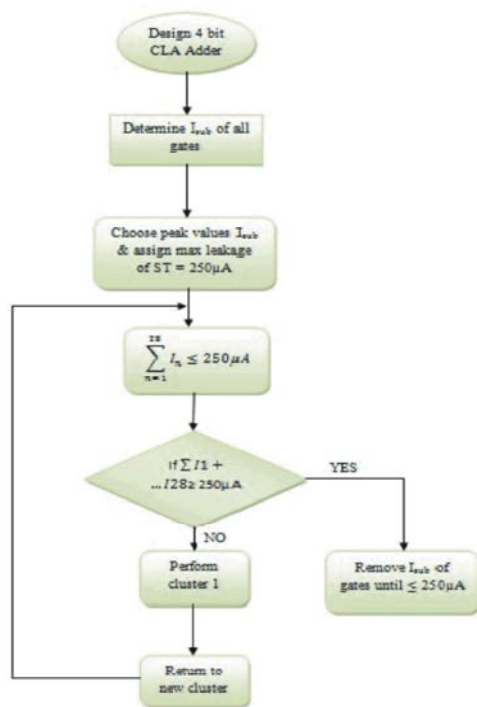


Fig. 3: Flow Chart Representation to Form Clusters

In this paper, 4 bit CLA adder is chosen as a conventional CMOS design [11]. The proposed clustering technique is experimented in 4 bit CLA adder by using Tanner Tool 15.1. Initially, schematic of CLA adder design is performed by using s-edit. By using T-spice coding, sub-threshold leakage of all gates (28) are determined in the design and the highest discharging value of each gate is filtered. Now, the proposed clustering algorithm is initialized in the schematic circuit in order to form cluster in the same design.

Power Gating: Power Gating is one of the methods used in IC design to reduce static power consumption, by shutting OFF the currents to block of the circuit that is not in use and also it is an effective approach to minimize standby leakage even though keeping high speed in the active mode. The most accessible way of reducing the leakage power dissipation of a VLSI circuit in idle mode is to remove its supply voltage. Power gating is the most effective solution to lower the leakage which is based on the principle of adding devices called sleep transistors [9], [12]. This can be disconnected from the power supply and/or ground to lower leakage in sleep mode. More accurately, this can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic circuit to create a virtual ground and a virtual power supply as depicted in Fig 4. Generally, an external switched power supply is a very basic form of power gating to achieve long term static power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. Typically, high threshold voltage sleep transistors are used for power gating, in a technique also known as multi threshold CMOS (MTCMOS). Also, the sleep transistor sizing is an important design parameter.

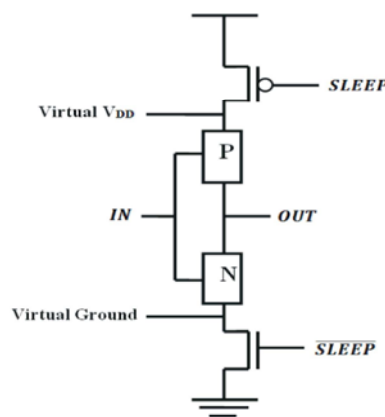


Fig. 4: Power Gating circuit

In the active mode, the sleep transistor is ON as a result, the circuit functions as usual. In the standby mode, the transistor is turned OFF, which disconnects the gate from the ground. To minimize the leakage, the threshold voltage of the sleep transistor must be large. Otherwise, the sleep transistor will have a large leakage current, which will make the power gating less effective [13]. Now, the sleep transistors are to be implemented in the group of clusters of design where the maximum leakage current is present. Thus the static power has been minimized by turning them ON during standby mode (SLEEP =1) and turning them OFF (SLEEP = 0) during working mode. Thus it results in more leakage savings with good performance.

RESULTS AND DISCUSSIONS

In this section, simulation results and comparisons against other existing techniques are presented.

4:1 MUX Using Sleep Approach: The target of the first subsection is to evaluate the existing power gating method. This is because the technique is widely used in low power VLSI systems for the purpose of reducing static power in idle mode even though the circuit provides high speed in active mode. Hence, we choose a conventional CMOS design. like 4:1 multiplexer [14] is chosen and it is implemented in S-edit using sleep approach and corresponding output waveform. Leakage power values are obtained by simulation as shown in Fig. 5, 6 and Table 1.

The simulation results of 4:1MUX shows that power gating is a very efficient approach to diminish leakage power in idle mode since, static power reduced is around 90% in 4:1 multiplexer while in standby mode. The count of sleep transistor is high for complex design which is the major drawback of this technique. Hence, clustering technique is introduced to reduce the sleep transistor counts and also determine the sub-threshold leakage of each cluster in the circuit design before using power gating.

4 Bit CLA Adder using Clustering: In the next experiment, it is targeted to evaluate the proposed clustering technique. For that, schematic of 4 bit CLA adder using S-edit is designed and output waveforms are obtained by simulating the circuit design as shown in Fig 7 and 8. After that, the sub-threshold leakage of all

gates (28) are measured by T-spice coding. Finally, clusters are formed based on proposed clustering algorithm and the clusters of 4 bit CLA adder is shown in Table 2.

Table 2 indicates that the sub-threshold leakage of cluster 5 is high while comparing to other clusters. Hence, sleep transistor is used in cluster 5 so as to shrink sub-threshold leakage and also to minimize static power in idle mode. Fig.9 shows the graphical representation of I_{sub} of cluster 5 with and without sleep transistor.

Table 3 clearly indicates that, the leakage power is reduced up to 75% with the use of two sleep transistors while using clustering technique and also it highlights that the reduction percentage is far better than before clustering i.e. 26% reduced Fig. 10 shows the bar chart representation of static power measurement of 4 bit CLA adder for clustering and non-clustering.

Moreover, delay is an important parameter in low power VLSI design and it should be taken into the consideration while designing low power systems. More aggressive techniques have been introduced with the purpose of reducing power, delay and other parameters in VLSI circuits. However, all the techniques will face up's and down's particularly if the techniques are focused to minimize all the parameters in digital circuits. In this paper, it is targeted to diminish static power of any conventional CMOS circuit in idle mode and the tabulated results show that the proposed approach is very efficient to reduce leakage power in standby mode. Nevertheless, delay is slightly increased around 1.4% due to the insertion of sleep transistor but it is not a major drawback because leakage is reduced to far better than any other existing techniques.

Delay calculation of 4 bit CLA adder and experimental results are shown in Table 4 and 5.

The proposed clustered power-gating methodology to 4-bit CLA adder is applied. The circuit was then synthesized and placed using a 45-nm CMOS technology library from PTM using Tanner Electronic Design Automation 15.1. Fig.11 shows the variation of Sub-threshold Leakage with number of clusters in 4-bit CLA adder. Fig. 12 shows the bar chart representation of static power measurement, delay in calculation and usage of sleep transistor counts for a cluster 4-bit CLA adder.

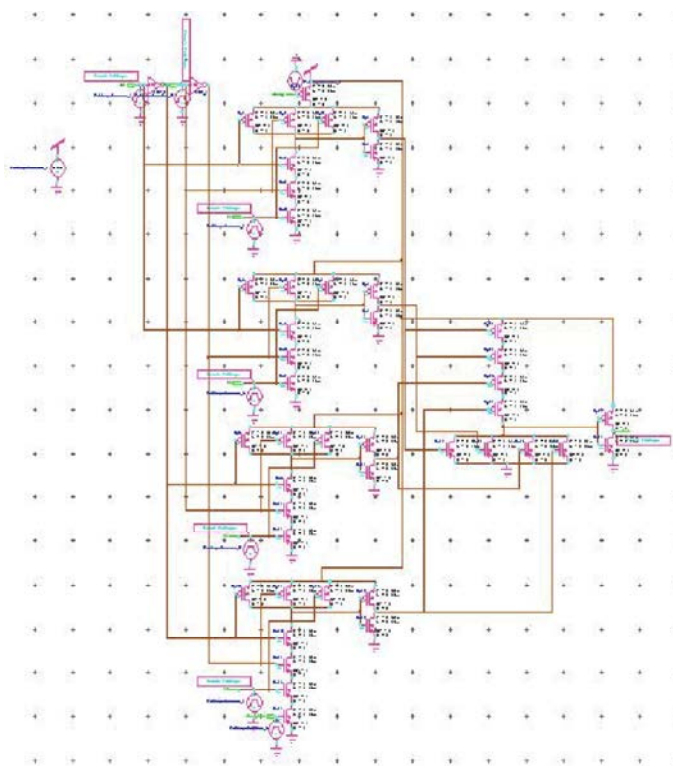


Fig. 5. 4:1 Multiplexer Using Sleep Approach

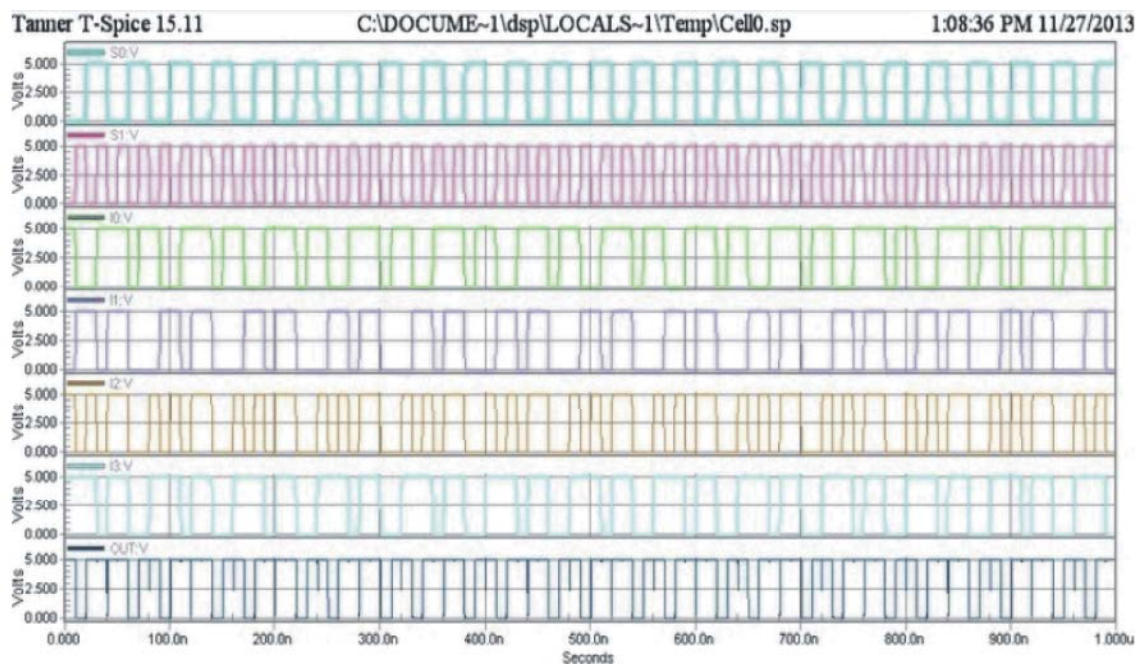


Fig. 6. Output waveform of 4:1 MUX

Table 1: Static power measurement

Parameters	With Sleep Transistor	Without Sleep Transistor
Static Power (μ W)	2.842344e-017 watts	1.272648e-011 watts

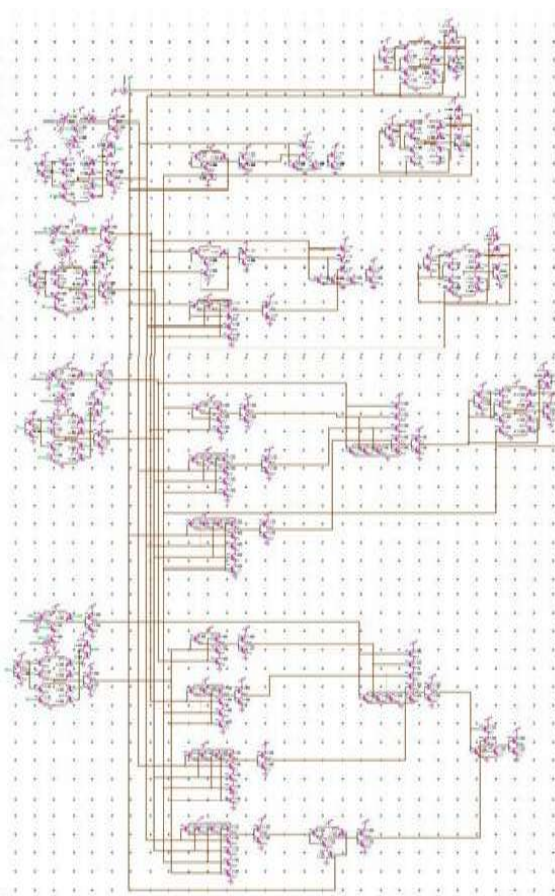


Fig. 8: Schematic of 4 Bit CLA adder

Table 2: Clusters of 4 Bit CLA adder

Cluster	Gates	Number of Gates	I_{sub} (Peak Value) Amps
1	G1, G9, G19, G24, G25	5	2.382×10^{-4}
2	G2, G3, G10, G11, G20, G26	6	2.401×10^{-4}
3	G4, G5, G12, G13, G14, G21, G27	7	2.383×10^{-4}
4	G6, G7, G15, G16, G17, G18, G22, G23, G28	9	2.396×10^{-4}
5	G8	1	2.416×10^{-4}

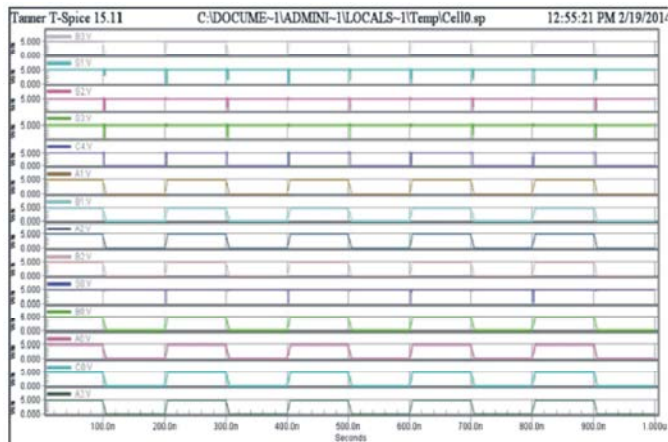


Fig. 9: Output waveform of 4 Bit CLA Adder

Table 3: Static power measurement using clustering

Voltage supply (2.5 V)		Without Sleep	With Sleep
Leakage Power (watts)	Before Clustering	2.104525×10^{-07}	1.556601×10^{-07}
	After clustering	2.966313×10^{-08}	7.482431×10^{-09}

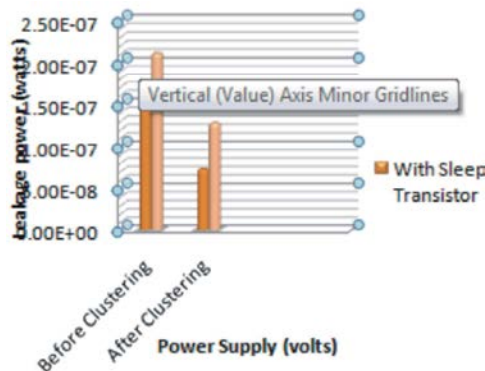


Fig. 10: Static Power Measurement with proposed technique

Table 4: Delay Measurement

Delay (seconds)	Without sleep	With sleep
	42.46ns	36.84ns

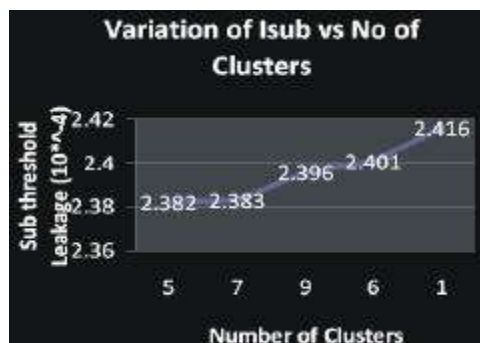


Fig. 11: Variation of Sub-threshold leakage with number of clusters

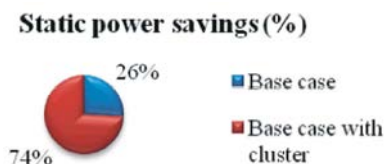


Fig. 12: Percentage of leakage savings

Table 5: Experimental Results: Clustering and Leakage Power Savings

Type	CMOS Design	Gates	Clusters	Sleep Transistors	Static Power	Delay	Leakage Savings (%)
Base Case	4-Bit CLA adder	28	-	-	2.104525×10^{-07}	42.46ns	-
Base case with Cluster	4-Bit CLA adder	28	5	2	7.482431×10^{-09}	36.84ns	74.17

CONCLUSION

As far as technology is concerned, leakage power has high impact on nanometer CMOS VLSI circuits. Over the past two decades, lots of design methodologies have

been invented with the purpose of diminishing leakage in hand-held portable applications. Anyhow, as scaling technology improves, leakage also increases and it seems as a critical factor in VLSI industry. In this paper, a modernistic approach with the aim of relegate leakage

power in low power CMOS VLSI circuits is proposed and the approach is implemented in 4 bit CLA adder using Tanner Tool 15.1. The same design is simulated using T-SPICE with and without clustering and leakage values are measured for the circuit with and without sleep transistor. This results in 74.77% reduction of leakage power in 4 bit CLA adder with sleep transistor. Since power gating is used only after finding the high leakage path in circuit design, sleep transistors are placed where the leakage is high. However delay gets slightly increased by 1.4% due to insertion of sleep transistors in 4 bit CLA adder.

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