# TRANSPORT PROPERTIES OF METALLIC NANOWIRES ON SILICON SUBSTRATE

By

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*ABSTRACT*

*This paper presents the electrical properties of the randomly distributed metallic (Co, Ni and Fe) nano/micro wires on Silicon. Deposition was carried out potentiostatically into the pores of the track-etch polycarbonate membrane spin coated onto the Silicon substrate. Spin coated films were irradiated with 150MeV Ni (+11) ions at a fluence of 8E7 ions/cm$^2$, followed by UV irradiation and chemically etching in aqueous NaOH (6N, at room temperature). Later morphological, and electrical properties of the so deposited nano-/micro structures were studied.*

*Keywords: Nanowires, SEM, Electrical Characterization*

## INTRODUCTION

The research on nano-/micro structures has led to the exploration of novel physics and material properties at reduced physical dimensions. There is considerable technological interest in the fabrication of arrays of high aspect ratio structures synthesized by electrodeposition for use as sensors and ultra-high-density information storage. Along with the synthesis of bare nano/micro structures, fabrication of one-dimensional nanostructures, or nanowires on the substrate (metallic or semiconducting), has been under intense investigation due to their lucrative device applications (Duan X., Huang, Y., Cui, Y., Wang, J., and Lieber, C.M., 2001, Chakarvarti, S. K., Vetter, J., 1993, Chakarvarti, S.K., Vetter, J., 1998).

In the present work, the track-etched membrane is used to synthesis nano-/micro structures on the substrate itself. Structures are grown directly over the semiconducting substrate for their further characterization and obviating the need for post- synthesis manipulations. These semiconductor based nano-/micro structures are expected to have practical applications in electronic circuit integration (Hirschman, K.D., Tsybeskov, L., Duttagupta, S.P., Fauchet, P.M., 1996, Huang, M.H., Mao, S., Fieck, H., Yan, H., Wu, Y. , Kind, H., Weber E., Russo, R., Yang, P., 2001). A thin polymeric layer was spin coated on the gold-coated semiconducting substrate. This gold layer acts as an electrode at the time of electrodeposition and polymeric layer acts as a template having the etched tracks.

### 1. Experimental Details

Preparation of the substrate was carried out at Inter University Accelerator Center (IUAC), New Delhi, India, and the CSIO, Chandigarh, India. We have used Si (P-doped) (111) as a semiconducting substrate. To remove the dirt and oxide layer from the surface of the substrate Si, wafer was kept in trichloroethylene solvent at 70°C for 10 min and then immersed in 1% HF-acid for 1 min. Finally, wafer was rinsed using deionised water for 5 min.

A thin gold layer of thickness about 95.5nm was deposited using vacuum evaporation method, onto the Au layer and polycarbonate (Makrofol) was deposited by spin coating (at room temperature with spinning speed of 4000rmp) and the thickness of coated polymer was around 10µm. The adhesion of the polycarbonate film on the substrate was improved by the use of a primer (hexamethyledisilisazan), a chemical reagent $(CH_3)_3Si\text{-}NH\text{-}Si(CH_3)_3$ , consisting of ammonia substituted with two trimethylsilyl functional groups.

The prepared samples were irradiated at room temperature with 150 MeV $Ni^{+3}$ ions at a fluence of 8E7 at IUAC, New Delhi, India. Later, the irradiated samples were UV treated (365 nm, 150 W/cm2) for 20 minutes to increase the selectivity of the chemical etching thus favoring the formation of cylindrically shaped pores. Etching was

performed in a home made one-compartment cell with a NaOH aqueous solution at room temperature for a time up to 50 min. The supported films were then immersed in an acetic acid solution and rinsed with milli-Q water at room temperature for 5 min and were then dried with hot air. It must be noted that the pore size depends both on the conditions of the ionic and UV irradiation, and on the conditions during chemical treatment of the tracks like nature and concentration of the reactants, temperature during etching and, time duration for etching. UV exposure leads to photo-oxidation in the polycarbonate and is able to increase the track etch ratio by an order of magnitude (Chakarvarti, S.K., Singh, P., Mahna, S.K., Sud L.V., 1990).

Electrodeposition within these pores of the supported template was performed at room temperature in a conventional one-compartment cell, with a copper rod working as anode and a gold layer working as electrode (cathode). Electrodeposition of copper, iron and nickel was done by using the electrolytic solutions containing the following compositions: Cu ($CuSO_4 \cdot 5H_2O$, 125 g/L; $H_2SO_4$, 100 g/L), Fe ($FeSO_4 \cdot 7H_2O$, 120 g/L; $H_3BO_3$, 45 g/L) and Ni ($NiSO_4 \cdot 6H_2O$, 300 g/L; $NiCl_2 \cdot 6H_2O$, 45g/L; $H_3BO_3$, 45 g/L). The electrodeposition of copper nano-/microstructure was carried out for 20 minutes at 2 V (current 0.0410 to 0.0 645 A) at the temperature of 60° C. Similarly, microstructures of iron and nickel were fabricated at a potential difference of 2 volt for 15 minutes and current variation was ranged from 0.0280 to 0.360 A at 60° C. The deposition potential was applied using a power supply (Electromek INDIA, SAM-Model MR 85, 15 V) and the monitoring of current and potential drop across the cell was carried out using a digital multimeter (PHILIPS Digital Multimeter 1225). When the wire reaches the membrane surface, a cap starts to grow on top. At this point in time, the electrodeposition process is stopped, the substrate with nano-/micro wires was immediately removed from the electrolyte, rinsed with double-distilled water and ethanol, finally dried in dry air at room temperature and subjected to further analysis. The porous thin polycarbonate membrane was removed by dissolving it in dichloromethane for 10 minutes and was washed several times with double-distilled water.

## 2. Results and Discussion

In the present study we have carried out morphological and electrical studies of template synthesized nano-/micro structures. For morphological characterization, the fabricated nano-/micro structures were viewed under SEM (Scanning Electron Microscope) at SEMCF IIT New Delhi. Figure. 1 shows the SEM images of Copper, Iron and Nickel nano/micro wires grown on the semiconducting substrate.

The in- situ I-V characteristics of nano-/micro structures was carried out at room temperature by leaving the structures embedded in the insulating template membrane itself . A KEITHLEY 2400 source meter was used for the measurement. Figure 2 shows the voltage vs current characteristics for the nano-/micro structures, which is the collective behavior of nanowires lying parallel to each other.

Plot shows that the metal- semiconductor contact system behaves non-ohmic when forward biased but in reverse biased region, the variation is ohmic.

Under forward biased V, at a fixed temperature T,

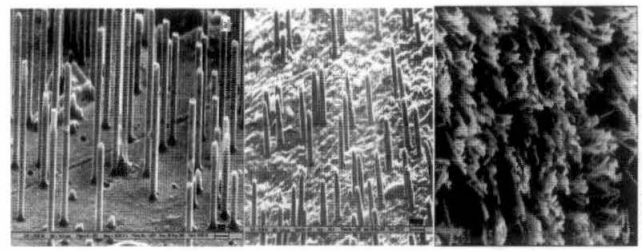

Figure 1. SEM image of (a) copper (b) iron and (c) nickel nano-/micro wires grown on silicon substrate.

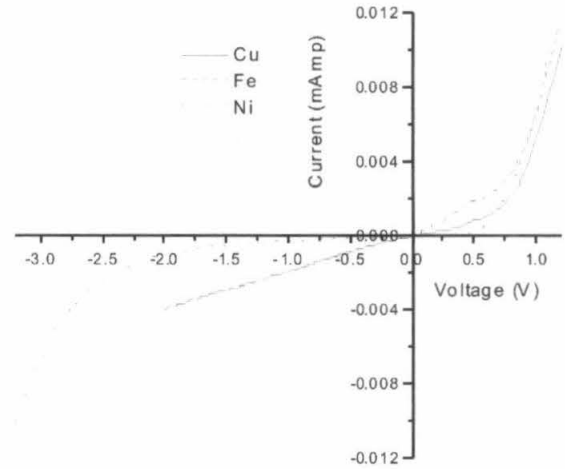


Figure 2. I-V characteristics of embedded nano-/micro copper, iron and nickel wires on Silicon substrate.

| Metal | Slope(mA/Volts) | Intercept (Amps) |
|---|---|---|
| Cu | 2.22 | 14.38 |
| Fe | 1.24 | 12.78 |
| Ni | 2.62 | 11.50 |

Table 1. Table showing the slope intercept and spreading resistance values for the nanostructures grown on semiconducting substrates.

$$I = I_0[\exp\{(q(v-IRs)/nkT)-1\}] \quad (1)$$

Where n is the ideality factor and $R_s$ is the diode series resistance. For a pure thermionic emission n=1, fit of linear region of the forward biased semilog IV curve (where $V>3k_BT$ and $R_s$ is negligible. Extrapolation of straight line portion of the plot to V=0 gives $I_0$ and the slope S=d(lnI)/dV gives n.

Using $I_0$ barrier height may also be calculated using the equation

$$\Phi_B=(kT/q)(AA^*T^2/I_0) \quad (2)$$

Where A* is the Richardson constant and A is the electrical contact area (Sze, S. M., 1981)

As the plots show the measured I-V curve is non-linear, Sze (1981) asserted that if thermionic emission is dominant, which is the major current flow mechanism for low impurity concentration, the curve should be linear. Padovani and Stratton (Padavani, and Stratton, R., 1966) reported that even if thermionic-field emission is dominant, which occurs at a highly doped metal semiconductor interface, the I-V curve is approximately linear (Pan, S. L. et.al., 2000). While Lepselter and Andrews (Lepselter, M.P. and Andrews, J.M., 1969) explained that if direct tunneling is dominant, the current is directly proportional to applied bias which implies that the contact is ohmic. However, our results indicate that the contact does not follow any of the three models. (Table1)

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### References

[1]. **Duan X., Huang, Y., Cui, Y., Wang, J., and Lieber, C.M., (2001).** "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices", *Nature London,* 409, 66-69.

[2]. **Chakarvarti, S. K., Vetter, J., (1993).** "Microfabrication of metal-semiconductor heterostructures and tubules using nuclear track filters". *Micromech. Microeng.*, 3,57-59.

[3]. **Chakarvarti, S.K., Vetter, J., (1998).** "Template synthesis- a membrane based technology for generation of nano/micromaterials: a review". *Rad. Meas.*, 29(2),149-159.

[4]. **Hirschman, K.D., Tsybeskov, L., Duttagupta, S.P., Fauchet, P.M., (1996).** "Silicon-based visible light-emitting devices integrated into microelectronic circuits Nature", 384, 338-341.

[5]. **Huang, M.H., Mao, S., Fieck, H., Yan, H., Wu, Y. , Kind, H., Weber E., Russo, R., Yang, P., (2001),** "Room-temperature ultraviolet nanowire nanolasers". *Science* 292,1897-1899.

[6]. **Chakarvarti, S.K., Singh, P., Mahna, S.K., Sud L.V., (1990).** "Ultrasound effects on the electrolytically controlledetching of nuclear track filters(NTFs)" *Indian J Physics* A, 64A(3), 229-232.

[7]. **Sze, S. M., (1981).** *Physics of Semiconductor Devices,* 2nd ed. Wiley, New York, Chap. 5.

[8]. **Padavani, and Stratton, R., (1966).** "Field and thermionic-field F. A. emission in Schottky barriers" *Solid State Electronics,* 9, 695-707.

[9]. **Pan, S. L., Zeng, D.D., Zhang, H.L. and Li, H.L. (2000).** "Preparation of ordered array of nanoscopic gold rods by template method and its optical properties" *Appl. Phys. A* 70, 637-640.

[10]. **Lepselter, M.P. and Andrews, J.M. (1969).** "Ohmic Contacts to Silicon", *The Electrochemical Society Symposium Series,* New York 159-189.

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