ADVANCED REFERENCES AND CARRIERS BASED PWM IN NEW SYMMETRICAL VOLTAGE SOURCE INVERTER

By

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ABSTRACT

In general, Pulse Width Modulation (PWM) techniques of a Voltage Source Inverter (VSI) need a sinusoidal reference signal and triangular carrier signal to generate the required modulating signals for the desired output. Modifications in modulating techniques can be considered in two ways, namely modified reference and modified carrier. The existing multilevel carrier based Pulse Width Modulation (PWM) strategies have no special provisions to offer good quality output, besides lower order harmonics that are introduced in the spectrum, especially at low switching frequencies. This paper proposes a new topology of a cascaded multilevel inverter that utilizes less number of switches than the conventional topology with a symmetrical DC source 7- level inverter. Phase Disposition (PD) strategy for Sinusoidal, Trapezoidal and Triangular reference with Triangular, Saw-tooth and Inverted Saw-tooth carrier strategy are simulated with the proposed topology. The performance has been analyzed with MATLAB/SIMULINK. By comparing the various references with various carrier strategies, it is observed that Trapezoidal signal provides less THD and higher fundamental RMS output voltage.

Keywords: Total Harmonic Disortion (THD), Phase Disposition (PD), Pulse Width Modulation (PWM), Triangular Reference with Triangular Carrier (TRTC).

INTRODUCTION

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Such inverters synthesize a desired output voltage from several levels of dc voltages as inputs. The general concept of multilevel inverters involves utilizing a higher number of power electronics switches to perform the power conversion in small voltage steps. The small voltage steps lead to obtain the low harmonic distortion and switching losses, devices possessing low voltage ratings and higher efficiency. The main advantages of this approach are summarized as follows:

- They are suitable for medium to high power applications.
- They can generate output voltages with extremely low distortion and lower (dv/dt).
- Their efficiency is high (>98%) because of minimum switching frequency.
- They can operate with a lower switching frequency.
- They use semiconductor switches without transformer and dynamic voltage balance circuits.

It is being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. When the number of output levels increase, harmonics of the output voltage and current as well as Electro Magnetic Interference (EMI) decrease. Phase Disposition PWM methods with different reference and carrier signals are investigated to obtain better THD for the proposed 7-level topology. Multilevel PWM method is based on control degrees of freedom combination and their theoretical analysis are carried out in this work. Pulse width modulation is the basis for control in power electronics. The theoretically zero rise and fall time of an ideal PWM waveform represents a preferred way of driving modern semiconductor power devices. The rapid rising and falling edges ensure that the semiconductor power devices are turned on or turned off as fast as practically possible to minimise the switching transition time and the associated switching losses.

Kangarlu et al [1] proposed a new topology for sub-

multilevel inverter and then series connection of the sub-multilevel inverters is proposed as a generalized multilevel inverter. Lakshmi et al [2] describe two topologies with 9 switches and 7 switches with level shifting technique and uses 1 KHz SPWM pulses with a modulation index of 0.8. Nedumgatt et al [3] explain a new topology of a cascaded multilevel inverter with PWM techniques. Balamurugan et al [4] made a comparative study on unipolar PWM strategies for three phase five level cascaded inverter. Najafi et al [5] carried out a new topology with a reversing-voltage component which is proposed to improve the multilevel performance. Leon et al [6] introduced a generalized modulation technique for cascaded H-bridge converter based on a multidimensional control region. Shukla et al [7] deal two improved natural balancing strategies for FCMI under PD scheme, which use the same (n - 1) carrier signals as used in the standard PD scheme. Jing Zhao et al [8] proposed the novel method which can effectively reduce the number of devices switching on or off within broad modulation index range, consequently reducing switching losses, and remarkably reduce the amplitude of lower harmonics. Ahmed et al [9] present the symmetrical and asymmetrical inverter, both of which are very effective and efficient for improving the quality of the inverter output voltage. Shanthi et al [10] analyzed a carrier overlapping PWM method for single phase cascaded multilevel inverter. Geethalakshmi et al [11] made a performance evaluation of three phase's cascaded H-bridge multilevel inverter based on multi carrier PWM techniques. Jinf Huang et al [12] present redundancy involving all phases which is used along with per-phase redundancy to improve capacitor voltage balancing. Escalante et al [13] describe the requirements imposed by a Direct Torque Control (DTC) strategy on multilevel inverters which are analyzed. Tolbert et al [14] proposed two novel carrier-based multilevel PWM schemes that are presented which help to optimize or balance the switch utilization in multilevel inverters.

1. The Proposed Multilevel Inverter

The most important part in multilevel inverter is switches which define the reliability, circuit size, cost, installation area and control complexity. The number of required switches against required voltage levels is a very important element in the design. To provide a large number of output levels without increasing the number of bridges, a new modified cascaded symmetrical multilevel inverter is proposed in this paper. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics. The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches. For increasing voltage levels, the number of switches also will increase in number. Hence the voltage stresses and switching losses will increase and the circuit will become complex. By using the proposed topology, number of switches will reduce significantly and hence the efficiency will improve. The configuration and the principle of operation of the proposed inverter have been presented. Figure 1 shows the proposed symmetrical inverter.

Proper switching control of the auxiliary switch can generate half level of dc supply voltage. This paper proposes various techniques to eliminate lower order harmonics. In the H-bridge, switches in the same leg should not conduct simultaneously, appropriate gate pulses should be given in order to prevent short circuit condition. Table 1 shows the switching states and possible output voltage of the converter.

1.1 Modulating Strategies

Modulation techniques for voltage source inverters may be carrier based or carrier-less and open loop or closed loop. These modulation or control techniques for multilevel voltage source inverters are classified. Simulation

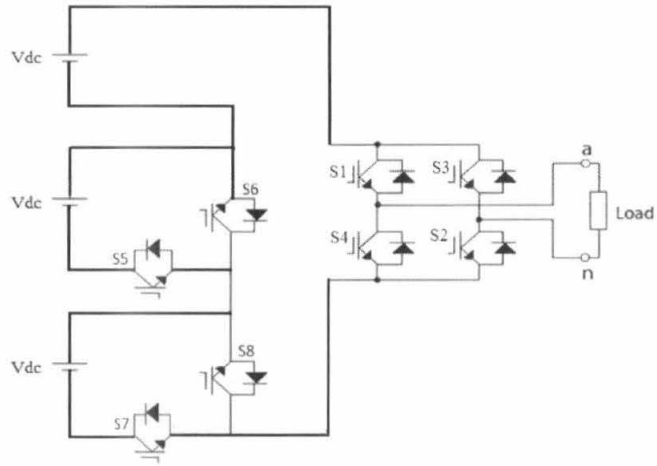

Figure 1. Schematic diagram of proposed symmetrical inverter

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	States
ON	ON	OFF	OFF	ON	OFF	ON	OFF	$3V_{dc}$
ON	ON	OFF	OFF	ON	OFF	OFF	ON	$2V_{dc}$
ON	ON	OFF	OFF	OFF	ON	OFF	ON	V_{dc}
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
OFF	OFF	ON	ON	OFF	ON	OFF	ON	$-V_{dc}$
OFF	OFF	ON	ON	ON	OFF	OFF	ON	$-2V_{dc}$
OFF	OFF	ON	ON	ON	OFF	ON	OFF	$-3V_{dc}$

Table 1. Switching state of proposed topology

investigation of different multilevel control techniques have been presented in this paper. Multilevel PWM techniques are extensions of two-level PWM methods; the multiple levels in these inverters offer extra degrees of freedom and greater possibilities in terms of devices utilisation and effective switching frequency.

The most popular PWM techniques for inverter are Phase Shifted Carrier PWM (PSCPWM) and Level Shifted Carrier PWM (LSCPWM).

1.1.1 Phase Shifted Carrier PWM (PSCPWM)

In general, a multilevel inverter with *m* voltage levels requires (*m*-1) triangular carriers. In the phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by $\Phi_{cr} = 360/(m\text{-}1)$. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves.

1.1.2 Level Shifted Carrier PWM (LSCPWM)

An *m*-level cascaded H-bridge inverter using level shifted modulation requires (*m*-1) triangular carriers, all having the same frequency and amplitude. The frequency modulation index is given by $m_f = f_{cr} / f_m$, which remains the same as that for the phase-shifted modulation scheme. The multilevel converter with multilevels requires (m_f) triangular carries with same amplitude and frequency. The frequency modulation index 'm_f' can be expressed as:

$$m_f = f_{cr} / f_m \qquad (1)$$

Where f_m is modulating frequency and f_{cr} are carrier waves frequency. The amplitude modulation index 'm_a' is defined by

$$m_a = V_m / V_{cr}(m\text{-}1) \qquad \text{for } 0 \leq m_a \leq 1 \qquad (2)$$

Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of each carrier wave. The amplitude modulation index, m_a is 1 and the frequency modulation index, m_f is 6. The triggering circuit is designed based on the three phase sinusoidal modulation waves V_a, V_b and V_c. Three of the sine wave sources have been obtained with same amplitude and frequency but displaced 120 out of phase with each other. The various techniques for level shifting carrier are given as: Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), Alternate Phase Opposition Disposition PWM (APODPWM), Carrier Overlapping PWM (COPWM) and Variable Frequency PWM (VFPWM)

1.2. Reference Signals

1.2.1 Sinusoidal Reference

They represent a class of periodic signals that are commonly used in many analysis techniques. Those involving Fourier series, decompose complicated waveforms into a series of sinusoidal waveforms. A sinusoidal waveform f(t) is usually represented by,

$$f(t) = A\cos(wt + \Phi) \qquad (3)$$

1.2.2 Trapezoidal Reference

It is a digital clock signal on an extremely important group of waveforms. This clock signals are often approximated as square waves, however, this is not very accurate. All real digital clock waveforms have a certain non-zero rise time, and a non-zero fall time.

1.3. Carrier Signals

1.3.1 Triangular Carrier

Both the leading edge and the trailing edge of the PWM output is modulated. The rising and falling edges of the triangle are usually symmetric so that the pulse is centred within a carrier cycle when the reference is a constant. The method is called constant –frequency double-edge modulation.

1.3.2 Saw-tooth Carrier

The leading (rising) edge of PWM output occurs at fixed instants in time while the position of the trailing (falling) edge is modulated as the reference signal level varies. Hence the method is also called constant-frequency trailing-edge modulation.

1.3.3 Invert Saw-tooth Carrier

The trailing (falling) edge of PWM output occurs at fixed instants of time, while the position of the leading (rising) edge is modulated as the reference signal level varies. The method is usually referred to as constant-frequency leading-edge modulation.

1.4. Simulation Results

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed PDPWM strategy for chosen proposed symmetrical inverter for various references like sinusoidal, trapezoidal, stepped and triangular signals and also for various carriers like triangular, saw tooth, invert saw tooth, sinusoidal and invert sinusoidal signals and corresponding %THD values are measured using FFT block and they are shown in Table 2. Table 3 shows the V_{RMS} of fundamental of inverter output for the same reference and carrier signals. Figure 2 shows the 7- level proposed topology. Figures 3-29 show the seven level output voltage of chosen proposed inverter and the corresponding FFT plots with various reference and carrier signals for Phase Disposition technique. It is also possible that this various reference and carrier signals are analysed with PD, APOD, POD, CO and VF. The figure below shows the simulated model with eight IGBT switch. In a practical scenario each of the switches requires a separate gate driver circuit. DC power source of 100 volts are used with a load of 10 ohms.

1.5. Sinusoidal Reference with various Carriers PWM strategy

- Sinusoidal Reference with Triangular Carrier PWM Strategy shown in Figures 3,4,5.
- Sinusoidal Reference with Saw-tooth Carrier PWM Strategy shown in Figures 6,7,8.
- Sinusoidal Reference with Inverse Saw-tooth Carrier PWM Strategy shown in Figures 9,10,11.

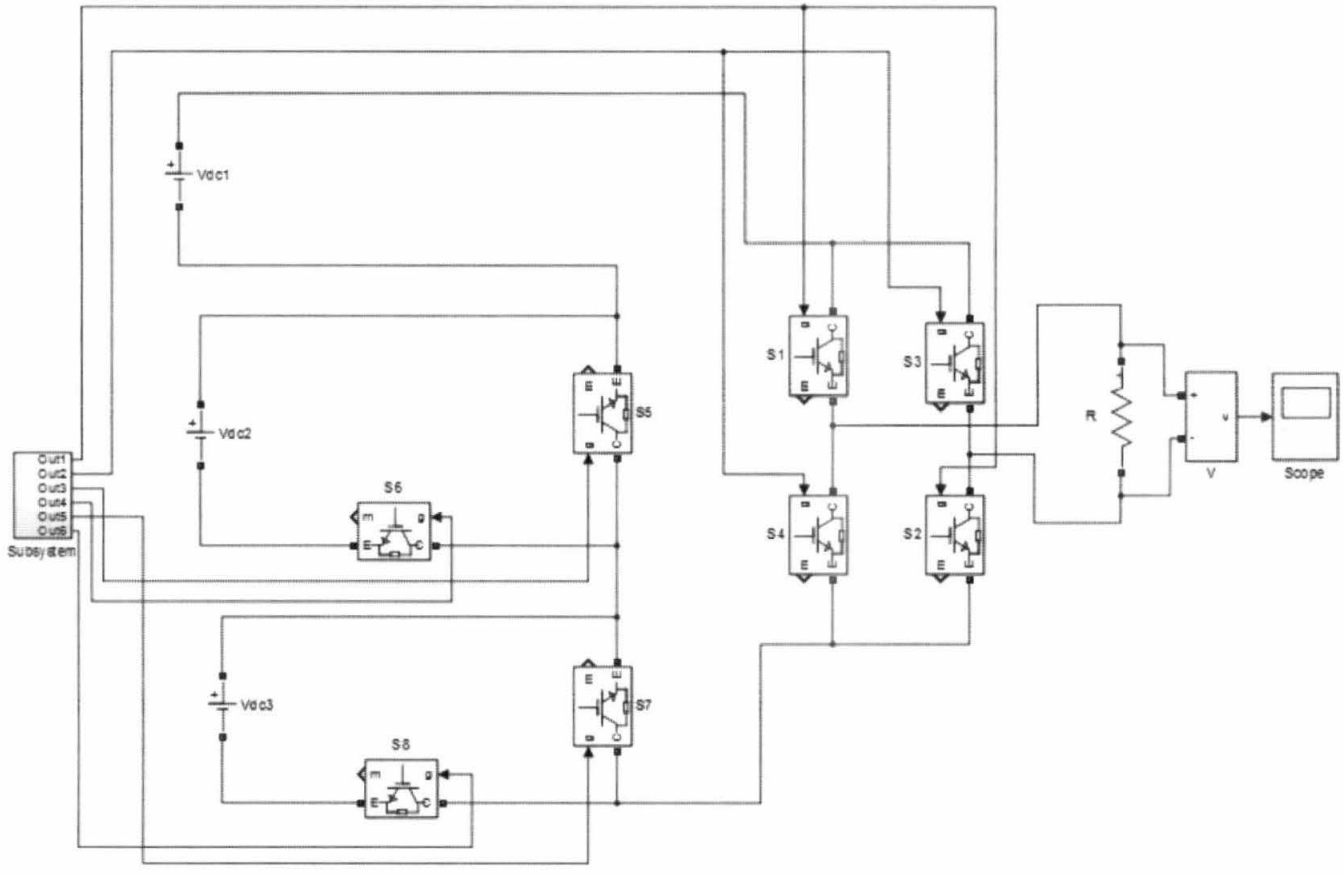

Figure 2. MATLAB/Simulink model of the 7-level proposed topology

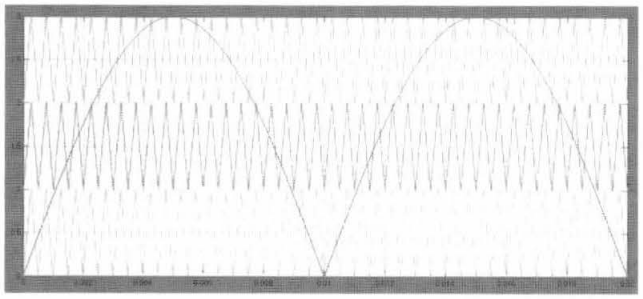

Figure 3. Sinusoidal References with Triangular Carrier (SRTC) waveform

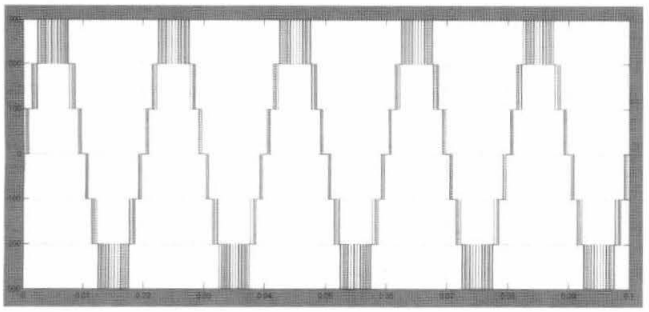

Figure 4. Simulated output voltage waveform for SRTC PWM strategy

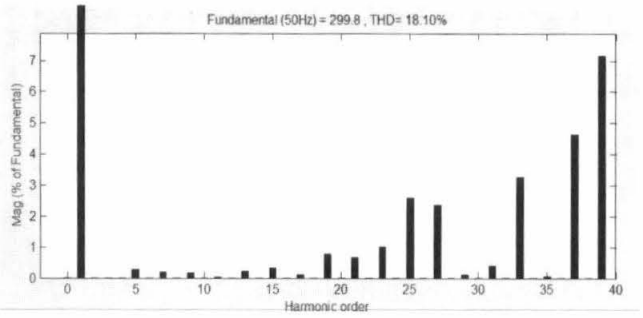

Figure 5. FFT plot analysis for SRTC PWM strategy

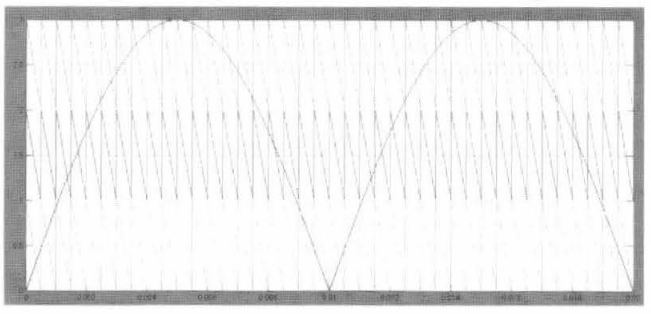

Figure 6. Sinusoidal References with Saw-tooth Carrier (SRSC) waveform

Reference	Triangular Carrier	Saw Tooth Carrier	Invert Saw Tooth Carrier
Sinusoidal	18.10%	17.67%	18.07%
Trapezoidal	16.83%	17.14%	17.04%
Triangular	26.56%	26.43%	26.87%

Table 2. Comparison of THD for various References and Carriers of Proposed Topology

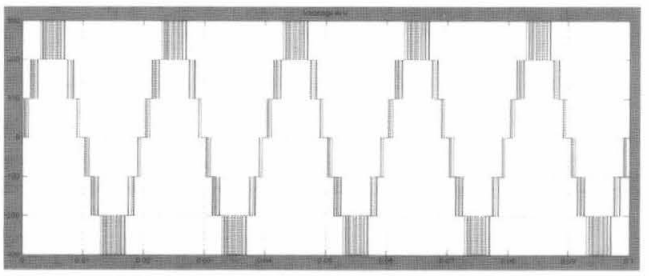

Figure 7. Simulated output voltage waveform for SRSC PWM strategy

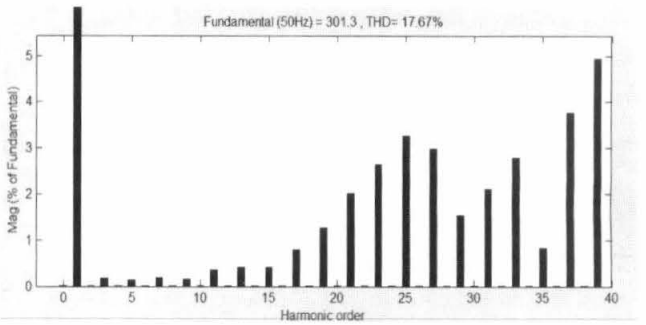

Figure 8. FFT plot analysis for SRSC PWM strategy

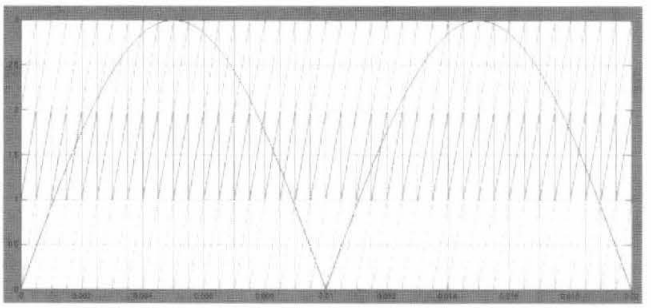

Figure 9. Sinusoidal References with Inverse Saw-tooth Carrier (SRISC) waveform

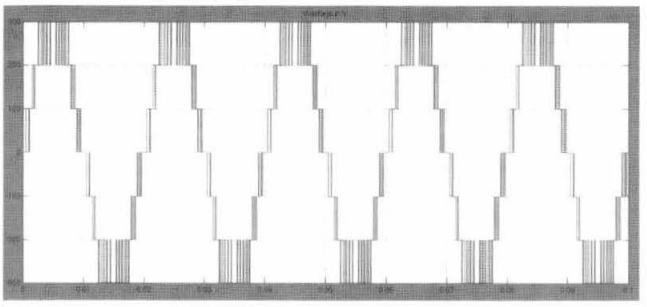

Figure 10. Simulated output voltage waveform for SRISC PWM strategy

Reference	Triangular Carrier	Saw Tooth Carrier	Invert Saw Tooth Carrier
Sinusoidal	212	213.1	211.4
Trapezoidal	243.3	244.1	243.8
Triangular	171.6	173.1	171.5

Table 3. Comparison of V_{RMS} for various References and Carriers of Proposed Topology

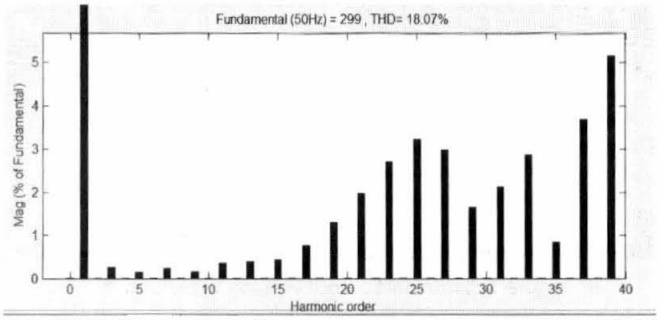

Figure 11. FFT plot analysis for SRISC PWM strategy

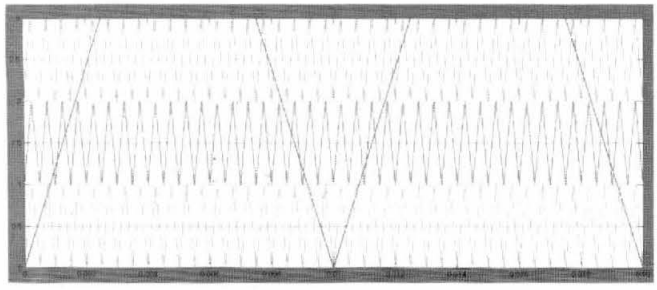

Figure 12. Trapezoidal References with Triangular Carrier (TRTC) waveform

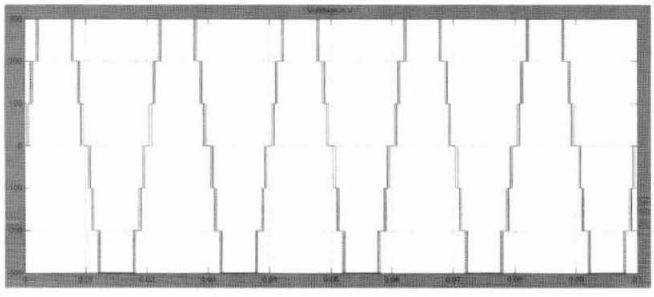

Figure 13. Simulated output voltage waveform for TRTC PWM strategy

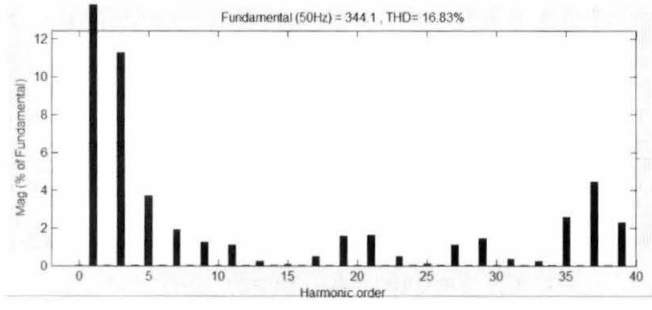

Figure 14. FFT plot analysis for TRTC PWM strategy

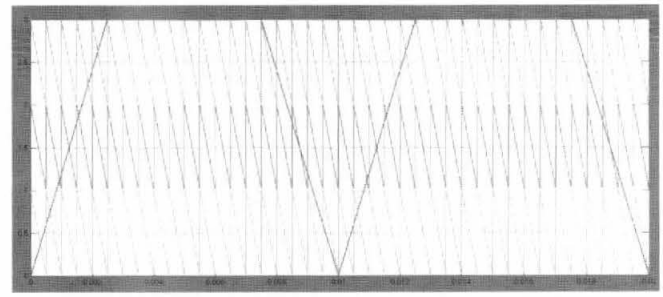

Figure 15. Trapezoidal References with Saw-tooth Carrier (TRSC) waveform

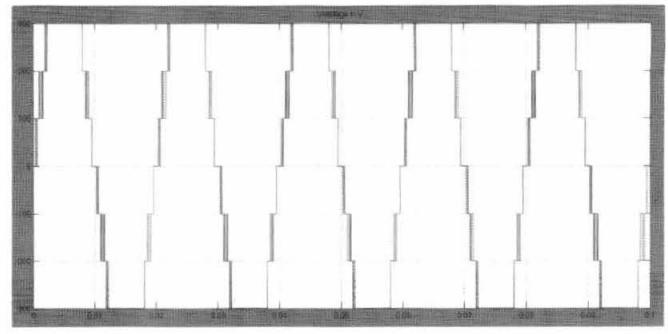

Figure 16. Simulated output voltage waveform for TRSC PWM strategy

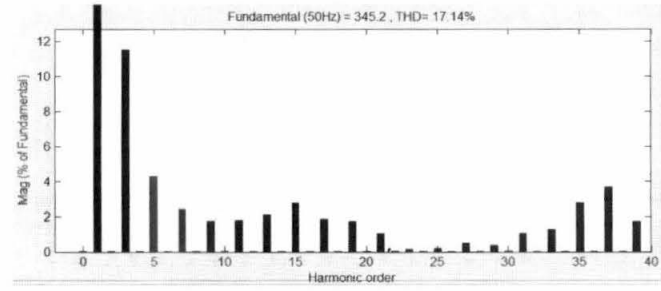

Figure 17. FFT plot analysis for TRSC PWM strategy

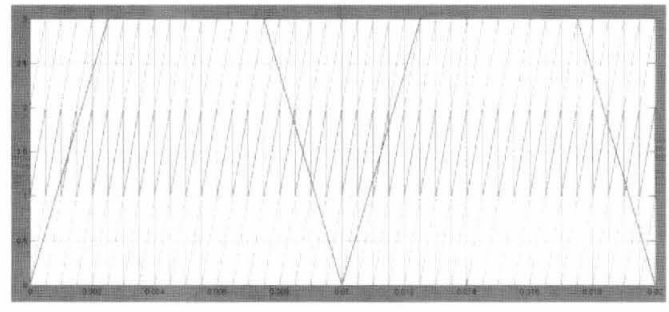

Figure 18. Trapezoidal References with Inverse Saw-tooth Carrier (TRISC) waveform

1.6. Trapezoidal Reference with various Carrier PWM strategy

- Trapezoidal Reference with Triangular Carrier PWM Strategy are shown in Figures 12,13,14.
- Trapezoidal Reference with Invert Saw-tooth Carrier PWM Strategy are shown in Figures 18,19, 20.

1.7. Triangular Reference with various Carrier PWM

- Triangular Reference with Triangular carrier PWM

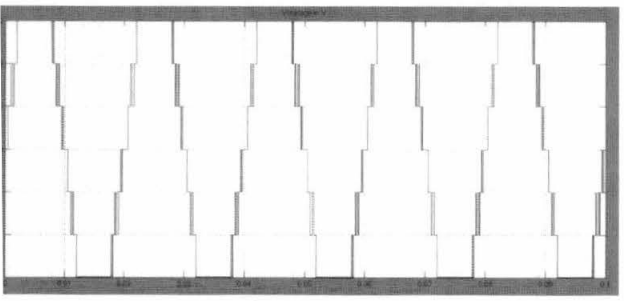

Figure 19. Simulated output voltage waveform for TRISC PWM strategy

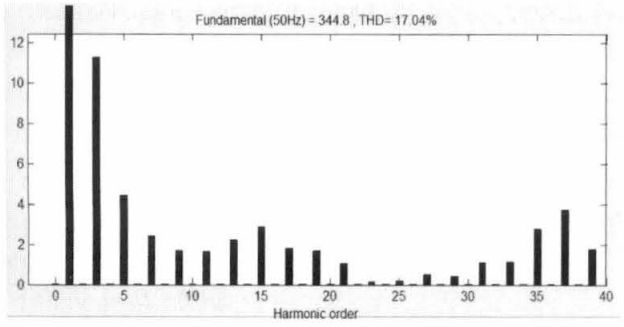

Figure 20. FFT plot analysis for TRISC PWM strategy

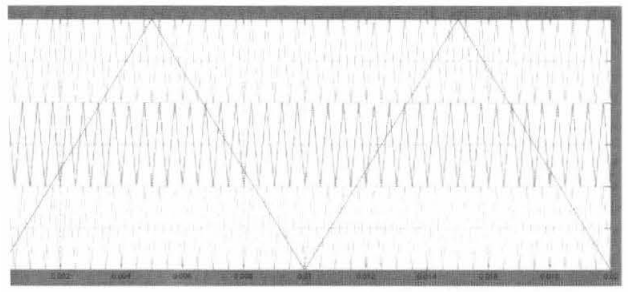

Figure 21. Triangular References Triangular Carrier (TrRTC) waveform

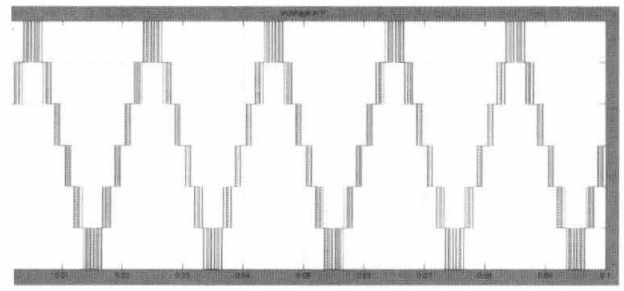

Figure 22. Simulated output voltage waveform for TrRTC PWM strategy

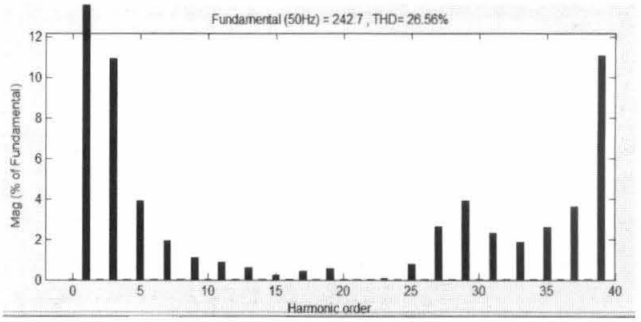

Figure 23. FFT plot analysis for TrRTC PWM strategy

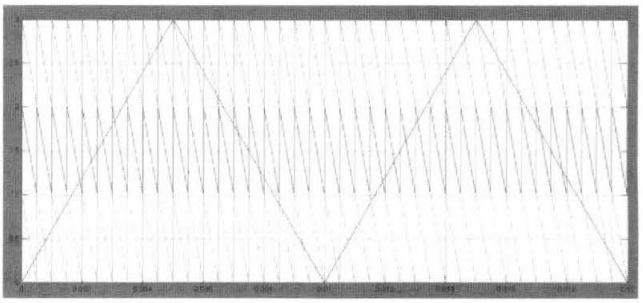

Figure 24. Triangular References with Saw-tooth Carrier (TrRSC) waveform

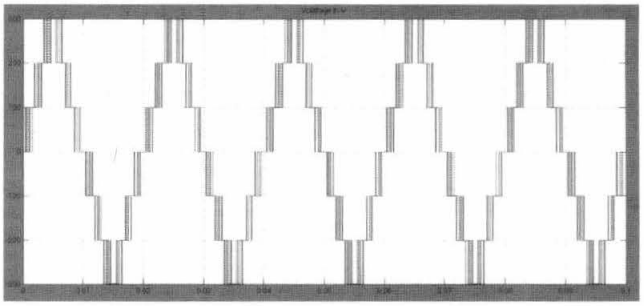

Figure 25. Simulated output voltage waveform for TrRSC PWM strategy

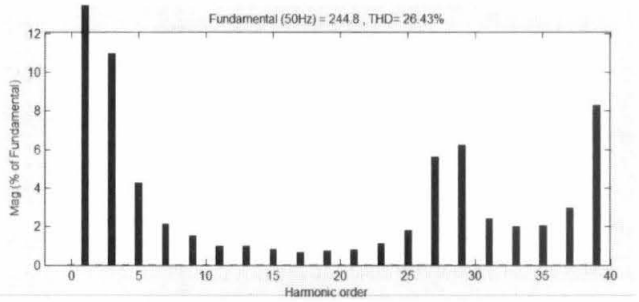

Figure 26. FFT plot analysis for TrRSC PWM strategy

Strategy are shown in Figures 21, 22, 23.

Triangular Reference with Saw-tooth carrier PWM Strategy are shown in Figures 24, 25, 26.

Triangular Reference with Invert Saw-tooth carrier PWM Strategy are shown in Figures 27, 28, 29.

Conclusions

In this paper, a new topology of the cascaded multilevel inverter has been shown to produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area reduces. Based on

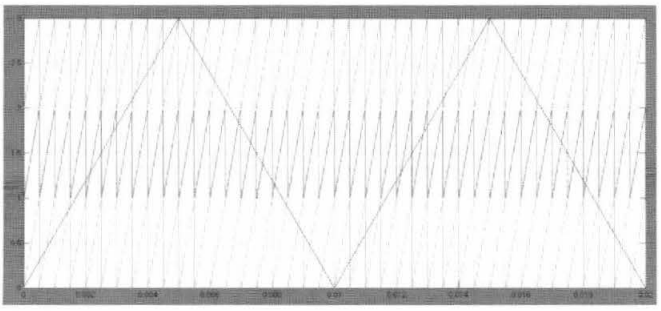

Figure 27. Triangular References with Inverse Saw-tooth Carrier (TrRISC) waveform

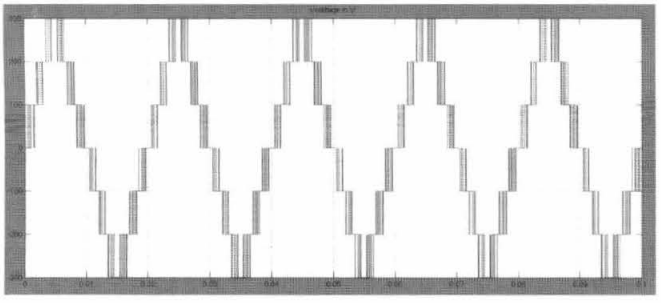

Figure 28. Simulated output voltage waveform for TrRISC PWM strategy

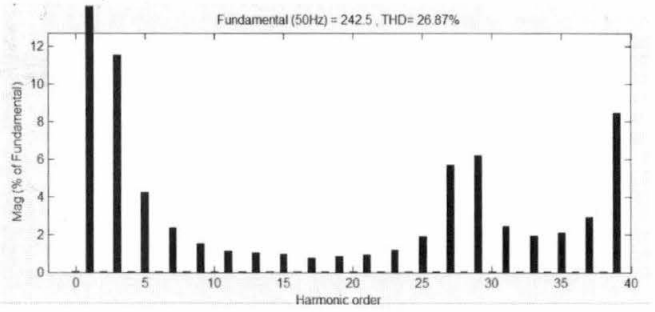

Figure 29. FFT plot analysis for TrRISC PWM strategy

the simulation results, UPDPWM techniques for proposed 7-level inverter have been presented for various references and various carrier signals. Performance factors like %THD, V_{RMS} have been evaluated, presented and analyzed. It is found that the Trapezoidal reference with Triangular carrier (TRTC) strategy provides lower %THD as in Table 2. Trapezoidal reference with Saw-tooth carrier (TRSC) strategy is found to perform better since it provides relatively higher fundamental RMS output voltage as in Table 3. Depending on the performance measure required in a particular application of chosen MLI based on the output quality, appropriate reference and carrier signals have to be employed.

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